FPGA in Advanced Vision Applications

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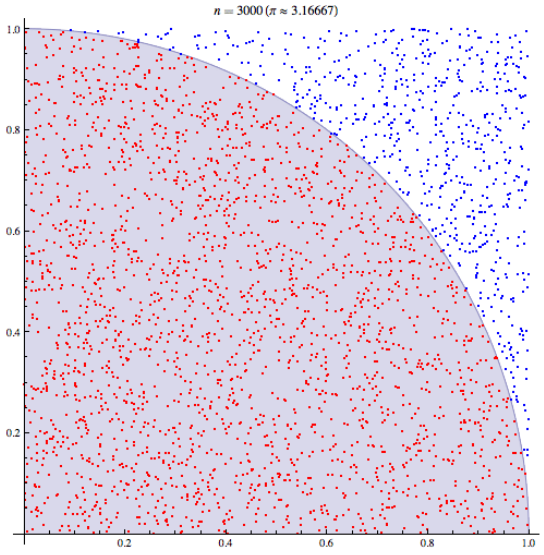
NATIONAL INSTRUMENTS

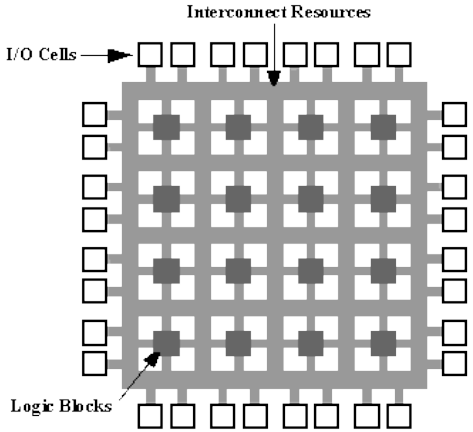
Multicore CPU systems

- Ride the CPU frequency wave
- Automatic hardware acceleration (SSE, Hyperthreading)
- Making software multithreaded
  - OpenMP (multiple cores)
  - MPI (multiple separate machines)
  - Vision Development Module
- Some problems divide well
- Others don’t

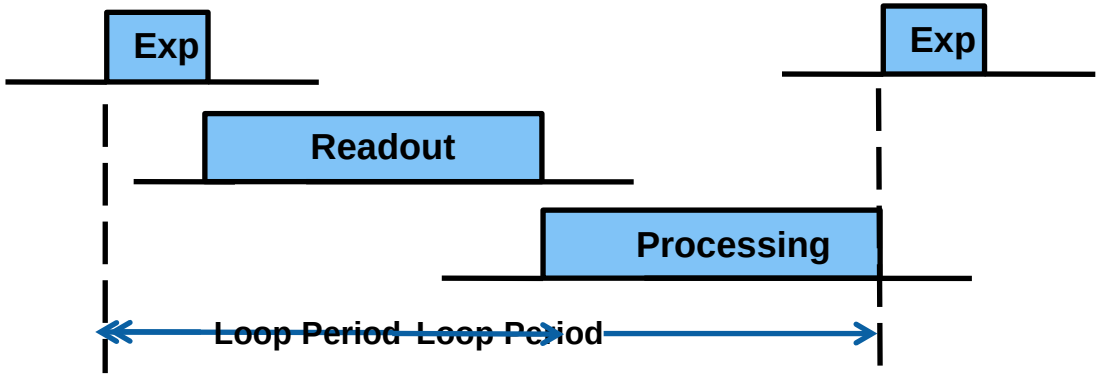


FPGAs

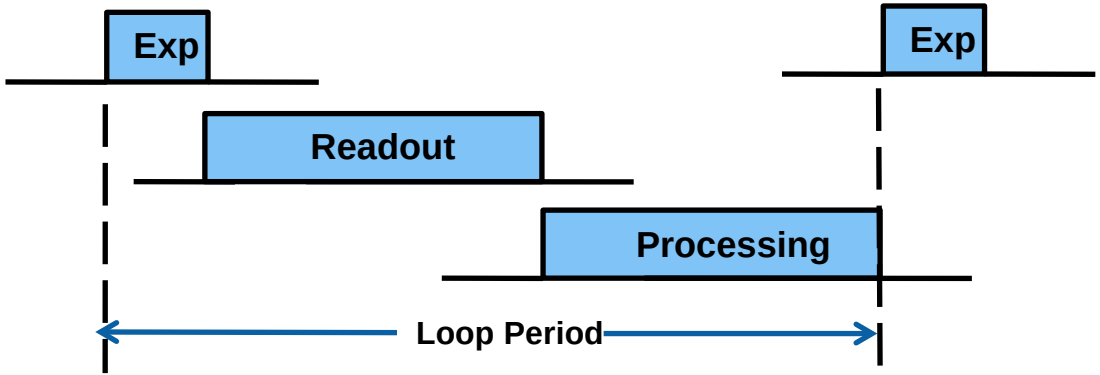
- Latency
- Jitter
- Compute power
- Pipelining
- Security
- Weight / Power / Heat
- Complexity
- Raw Clock Rates
- Limited Floating Point support



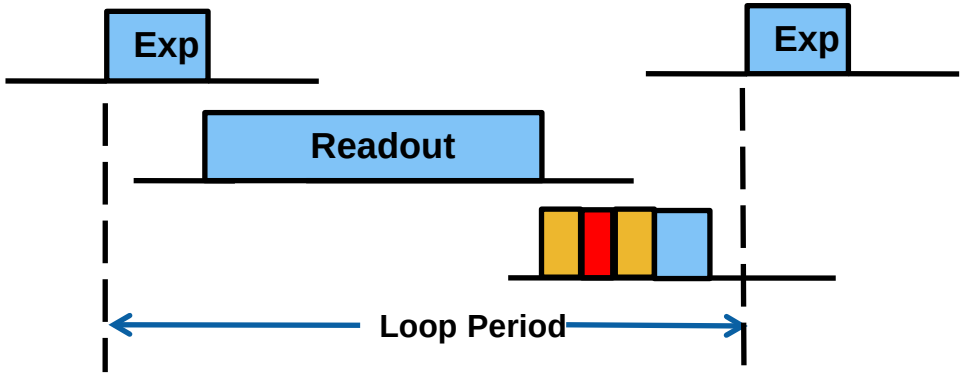
Latency - Preprocessing



Latency – Co-processing



Latency – Co-processing

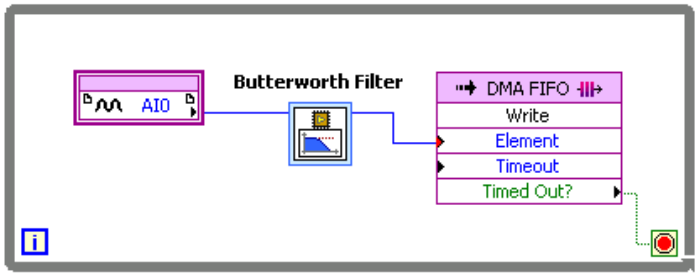


Complexity

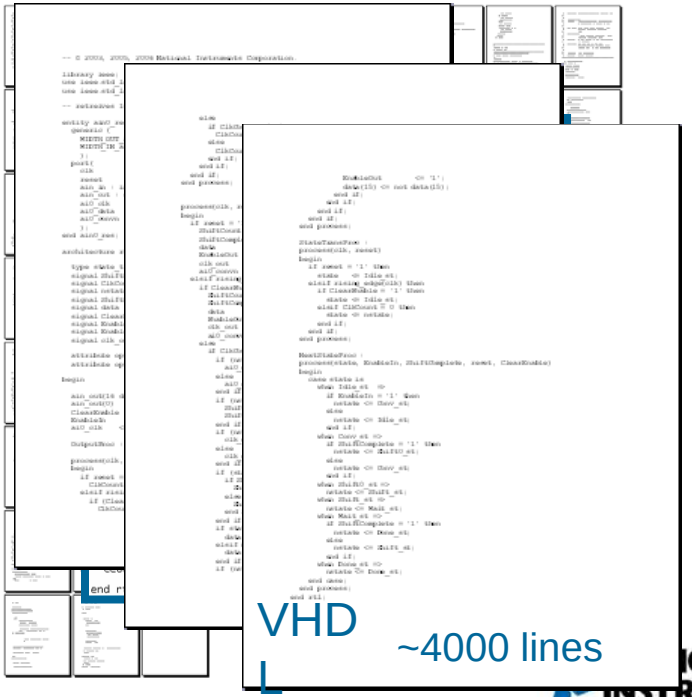
Counter

Analog I/O

I/O with DMA



LabVIEW FPGA



~4000 lines

FPGA Use Modes

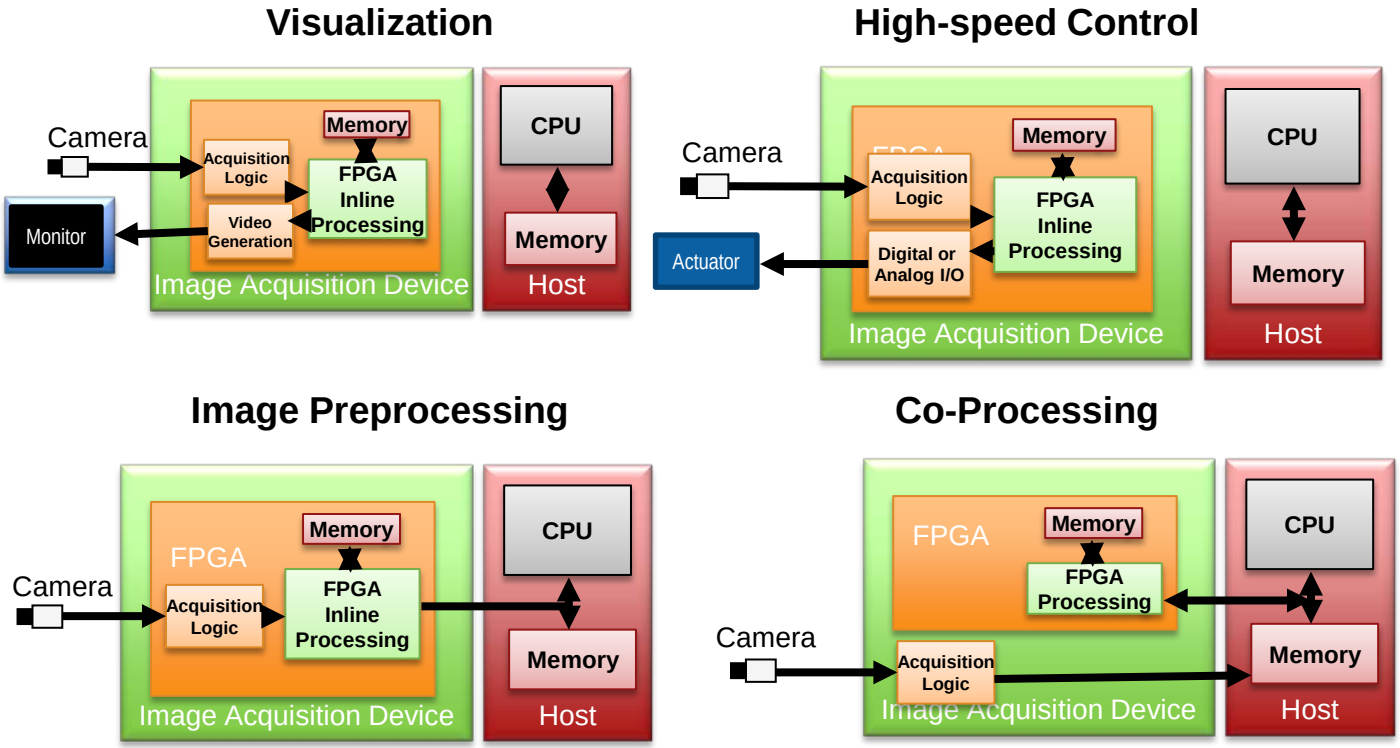
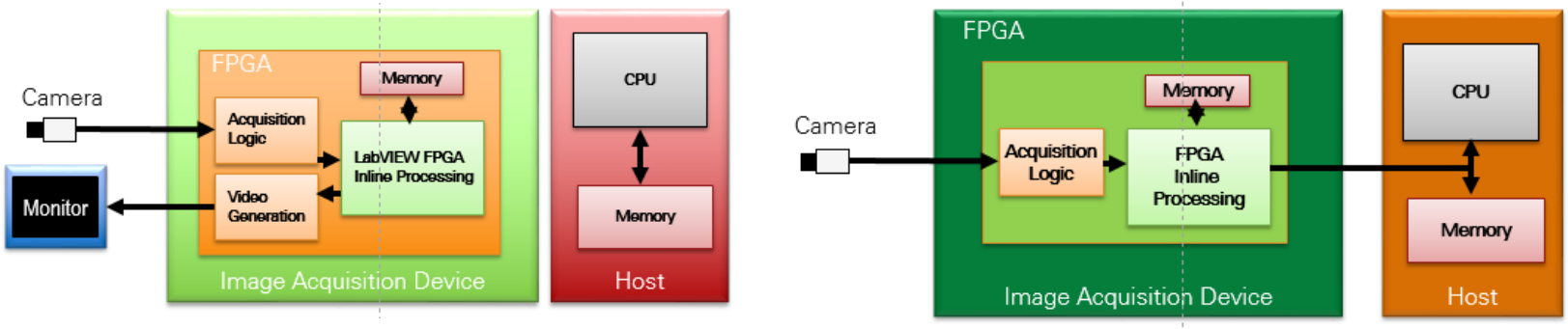


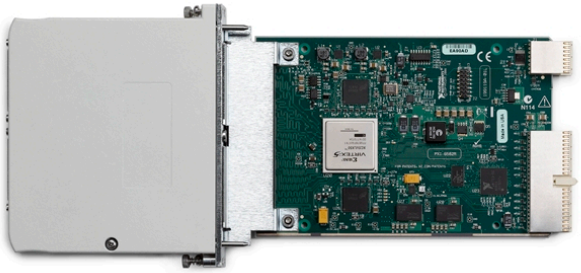
Image Processing and Visualization

- FPGA is directly in the path of the image data
- Processes pixels as they arrive
- May require some buffering—2D kernel operations
- Generates and outputs images directly or send result to host CPU

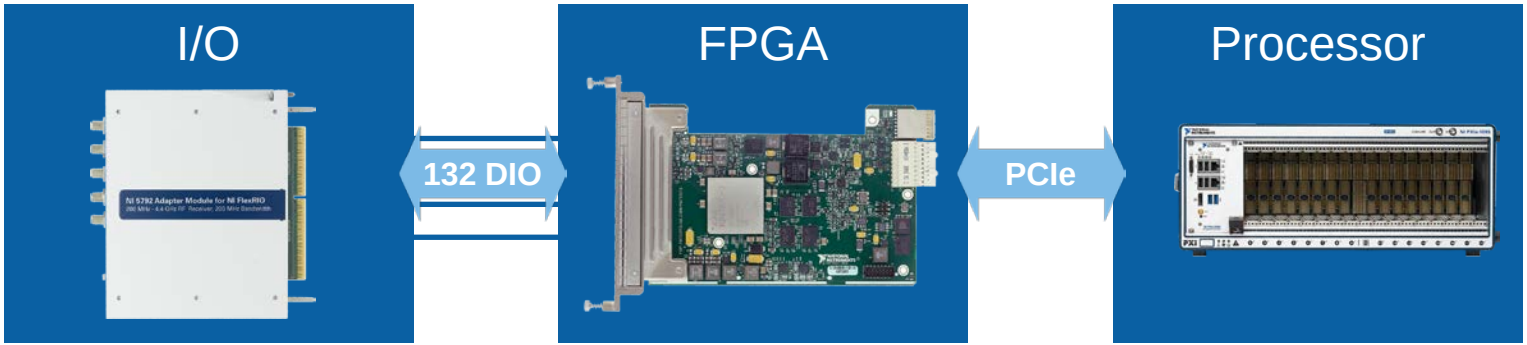


NI FPGA Hardware

- NI FlexRIO + NI 1483 adapter module
- PCIe-1473R
  - Base, medium or full configuration cameras
  - General purpose digital I/O
- LabVIEW FPGA example programs
  - Area scan and linescan image acquisition
  - Threshold
  - Centroid
  - Bayer decoding



FlexRIO for PXI System Architecture



FlexRIO Adapter Module

Camera Link Module

FlexRIO FPGA Module

Kintex-7 FPGA
Up to 2 GB of DRAM
PCIe Gen 2 x 8

PXI Platform

Embedded Controllers
Synchronization
Data streaming
Power/cooling

Visualization

- Image transformation
  - Image warping, rotation and flip
  - Image compression, encryption, and authentication
- Feature highlighting
  - Filtering
  - Shading correction
- Noise reduction
  - Image averaging
  - Retinex algorithm

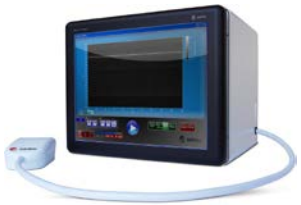


Image Processing Functions

FPGAs suitable to improve images and extract basic features

- Preprocessing
  - Image transforms
  - Image operators
  - Shading correction
  - Bayer decoding
  - Color space conversion
  - 1D & 2D FFT
  - Filtering (smooth/sharpen)
  - Binary morphology
- Feature Extraction
  - Edge, lines corners
  - Binary objects
  - Color
- Measurements
  - Centroid
  - Area measurements

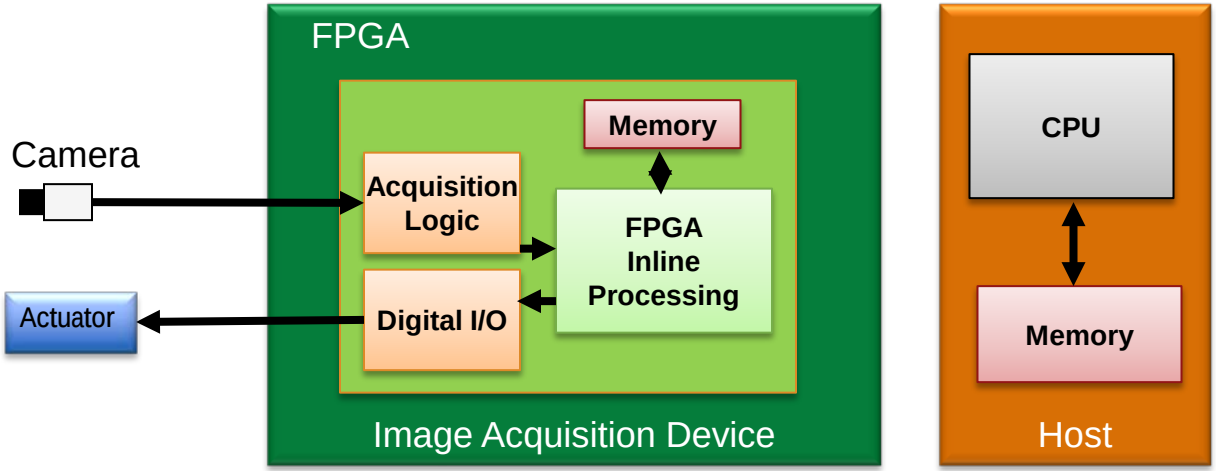
Image Processing Functions

FPGAs not suitable for certain high-level algorithms

- Object-level vision functions
  - Pattern matching
  - OCR/OCV
  - Barcode reading
  - Some geometric measurements
  - Classification

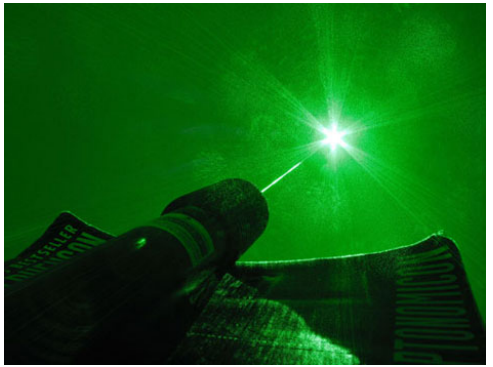
High-Speed Control

- FPGA is directly in the path of the image data
- FPGA generates and outputs control commands directly



High-Speed Control

- Laser alignment/steering
  - Beam profile/position measurements
  - Low latency control output
- High-speed sorting
  - Segmentation
  - Measure parameters of contaminant
  - Trigger rejection valves
- In Air Sorting
  - Image and inspect falling product
  - Low jitter requirement for decision making and IO



Example: Medical Imaging

Challenge

Develop the signal processing backend for an Optical Coherence Tomography machine.

High Level Requirements

Sample at 800 MS/s

Control fast steering mirrors to perform raster scan

Imaging in real-time

Stream image data over the network

FlexRIO Optimized for Deployment

FlexRIO Adapter Module

Interchangeable I/O
Analog, Digital, RF
Custom I/O with MDK

Controller for FlexRIO

Kintex-7 FPGA
Dual-Core ARM Processor
High Speed Serial
NI Linux Real-Time OS
Optimized for Size, Weight, Power

OCT Solution with Controller for FlexRIO

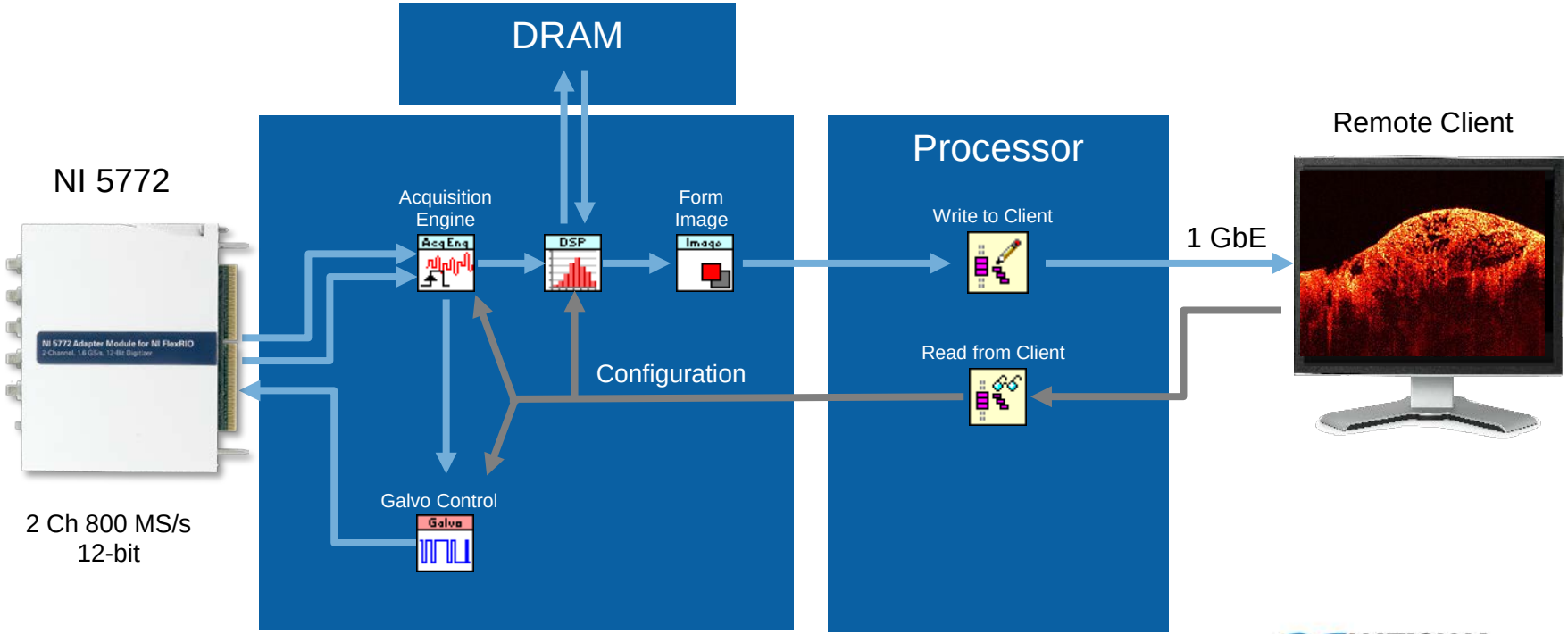
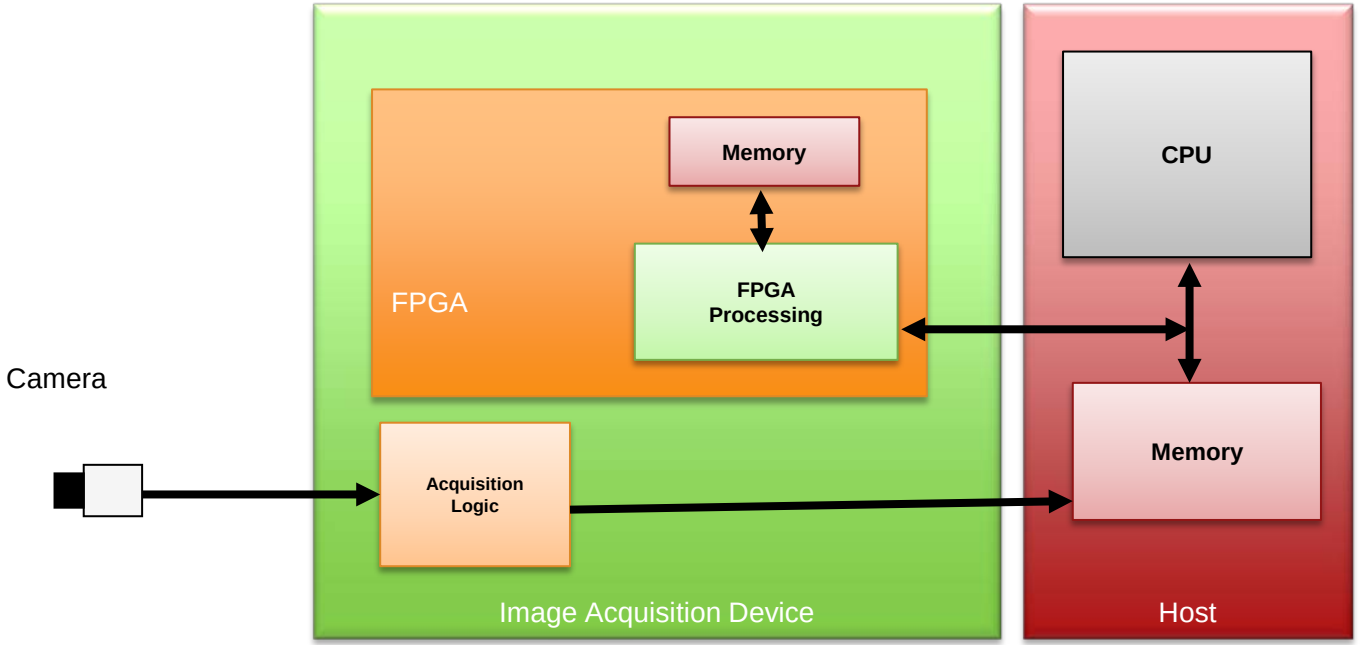
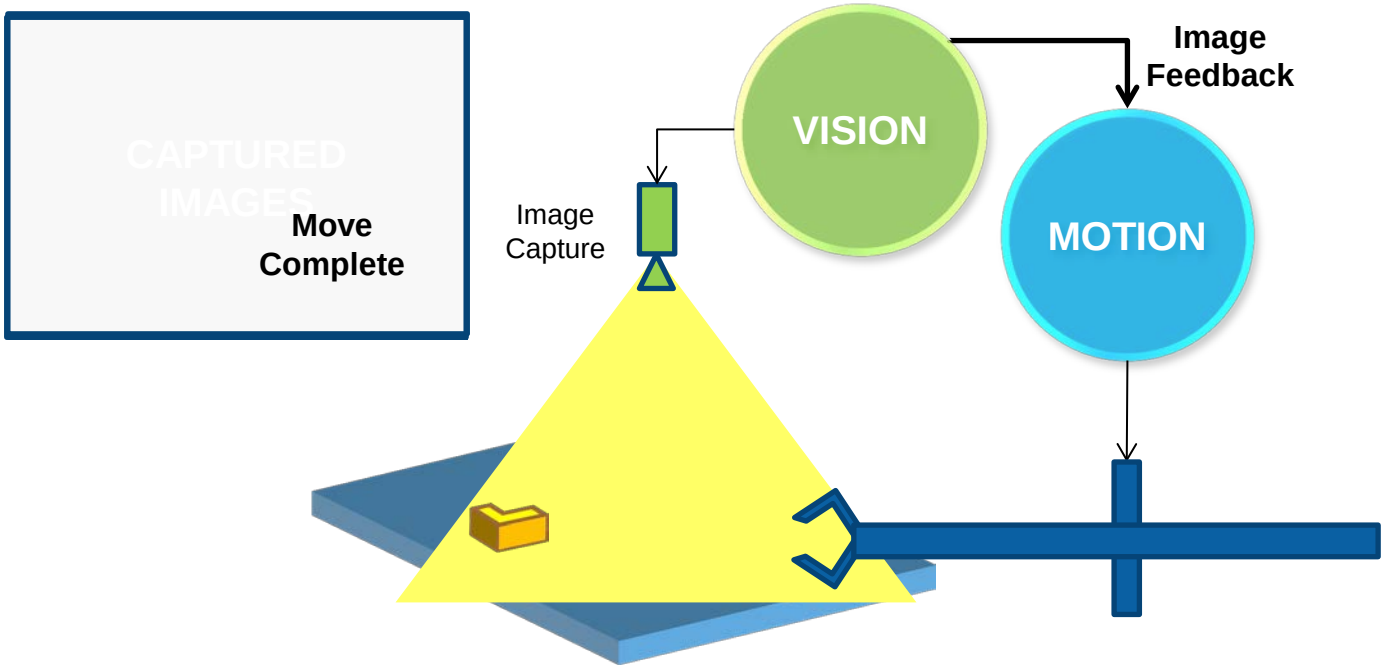


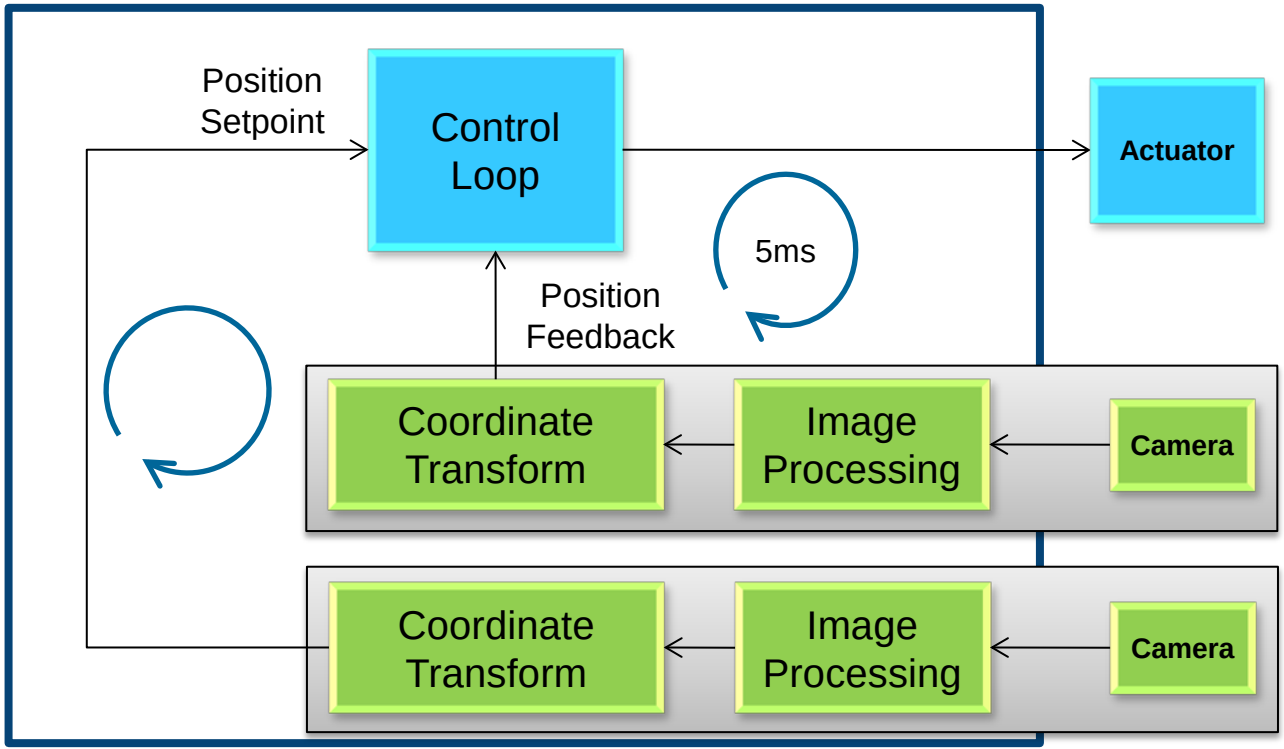
Image Co-processing



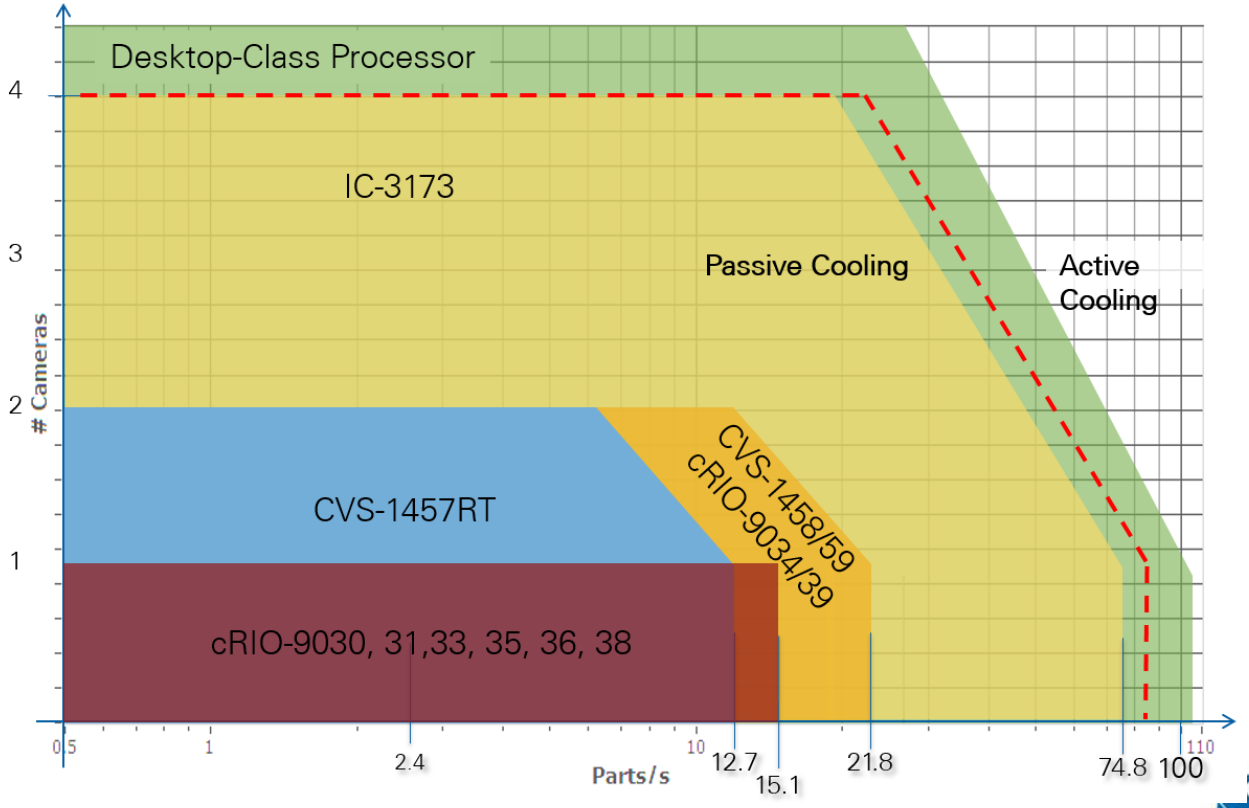
Visual Servo Control



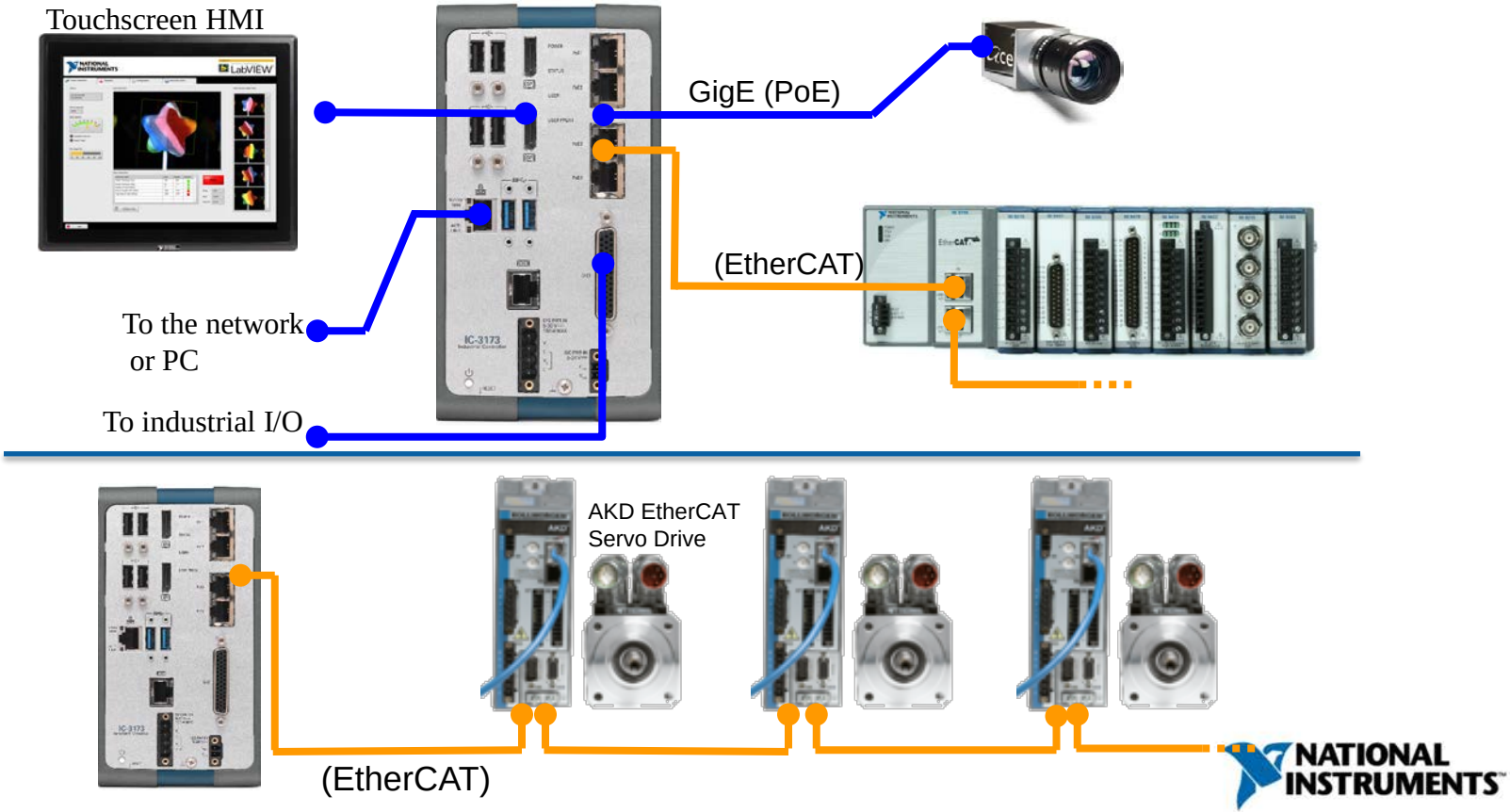
Visual Servo Control: Direct Servo



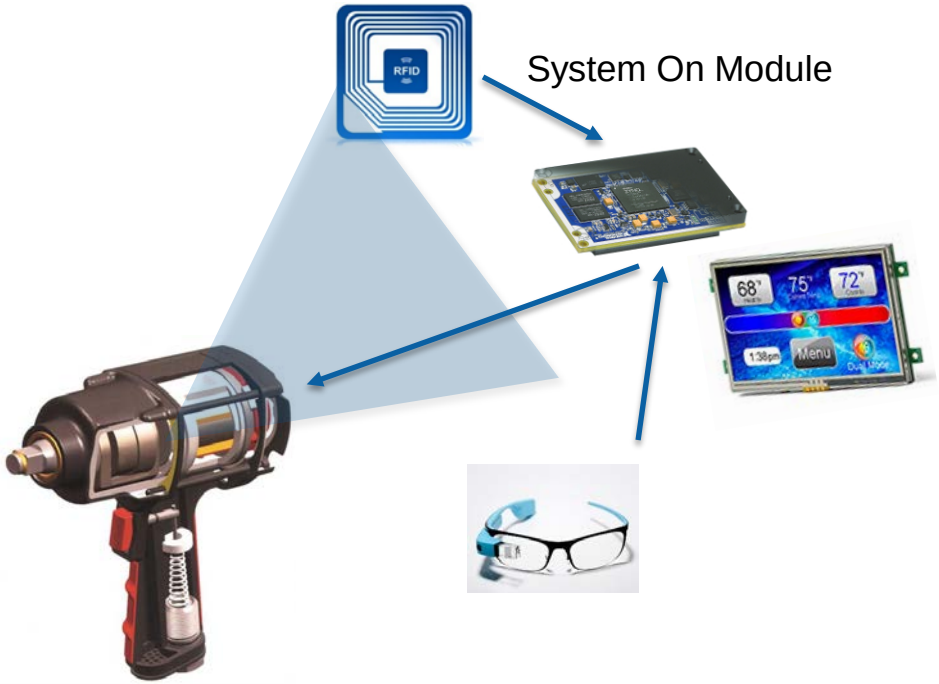
Target Performance Comparison Example



IC-3173 EtherCAT Master: Machine Controller



Future Looking Projects Using FPGA Co-processing



You Might Want to Use an FPGA for Vision…

- If latency or jitter is critical
- If power consumption is critical
- If you have to speed up throughput
- If you can pipeline your algorithms
- If you have to reduce the amount of data or aggregate multiple high-speed channels
- If you are using algorithms that can take advantage of the FPGA architecture
- If the FPGA is already in the image path
- If any of the above give you a competitive advantage