

# FPGA for image processing



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[www.ni.com/vision](http://www.ni.com/vision)



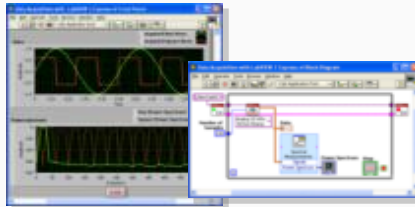
# National Instruments - What We Do

NI combines graphical programming software with modular hardware, leveraging the latest technologies.

Low-Cost Modular Measurement  
and Control Hardware



Productive Software  
Development Tools



Highly Integrated  
Systems Platforms

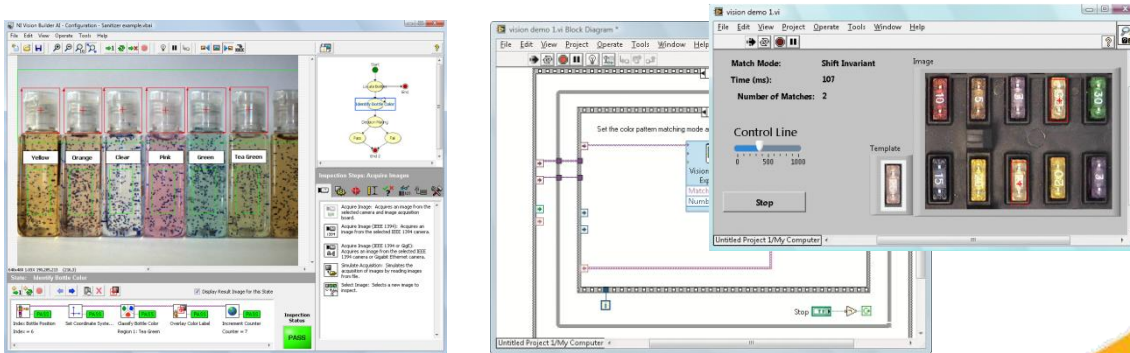


# Graphical System Design

A Platform-Based Approach for Measurement and Control



# NI Vision Platform



**Vision Builder for Automated Inspection  
Vision Development Module**

Smart Camera



Smart Cameras

Compact  
Vision System



Stand-Alone Vision Systems

Embedded  
Vision System



PXI Frame Grabber

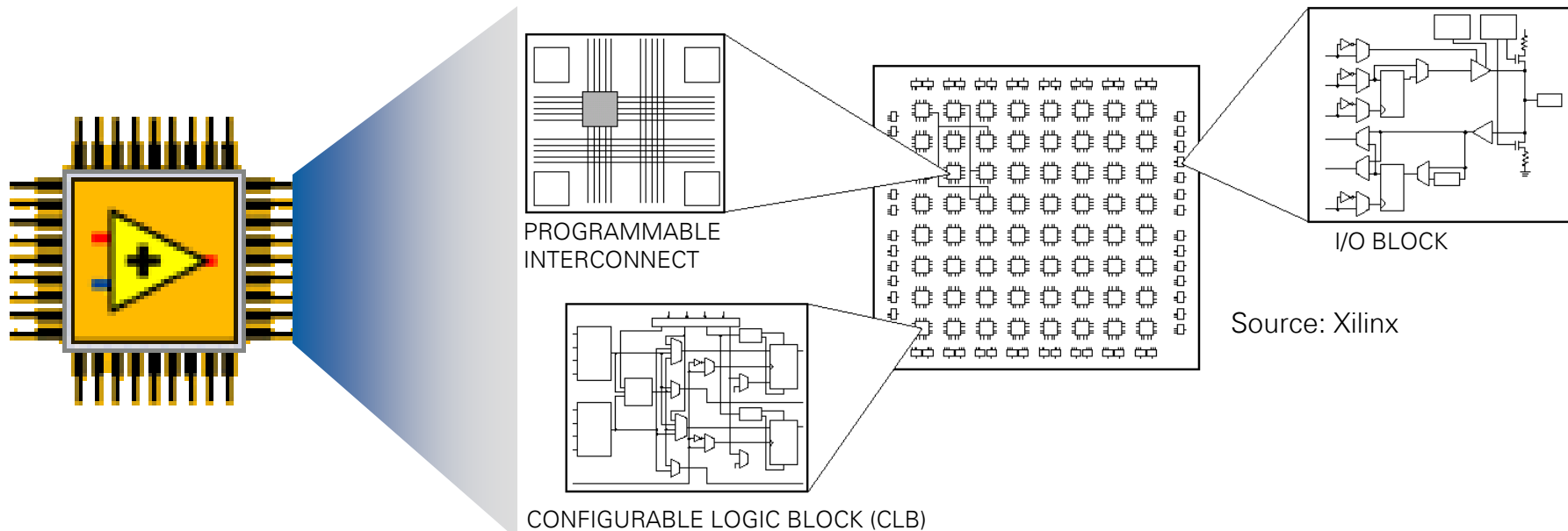


PC-Based Vision Systems

PCI and PCIe  
Frame Grabber



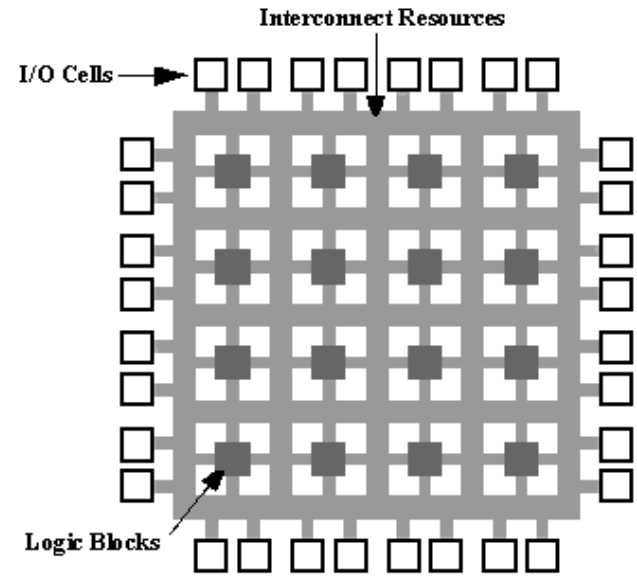
# Field Programmable Gate Array (FPGA)



- A semi-conductor device containing many gates (logic devices)
- A wiring list downloaded to the FPGA determines the gate connections and the functionality

# FPGAs

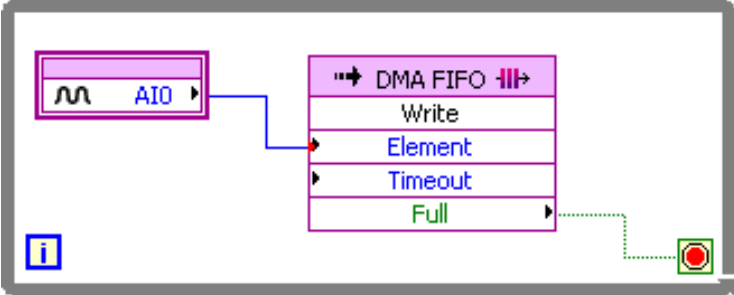
- Latency ✓
- Jitter ✓
- Compute power ✓
- Pipelining ✓
- Security ✓
- Weight / Power / Heat ✓
- Complexity ✗
- Raw Clock Rates ✗
- Limited Floating Point support ✗



# LabVIEW FPGA - Abstraction to the Pin



VHDL

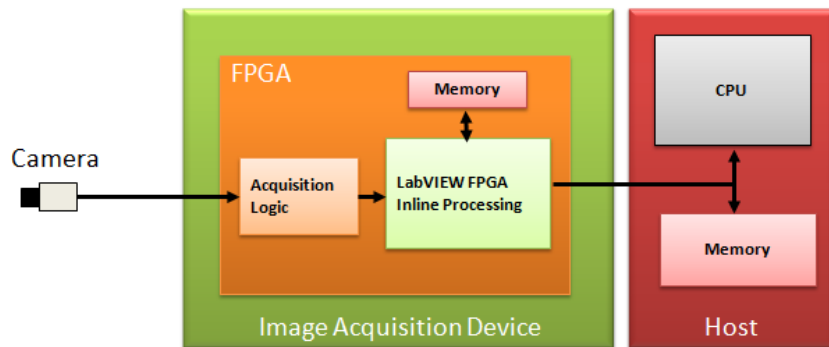


LabVIEW FPGA



# FPGA Image Processing

- High-speed control

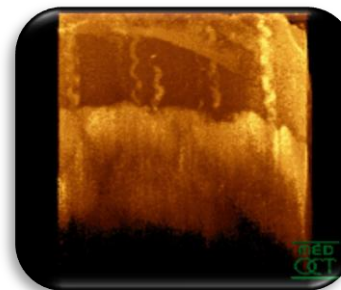
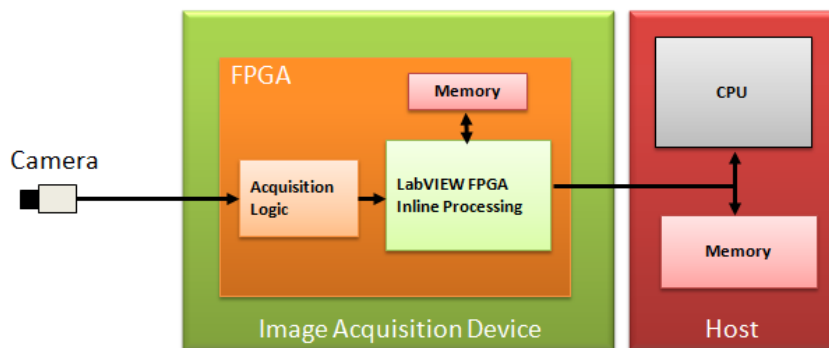


Laser Alignment & Tracking



High-Speed Sorting

- Image pre-processing



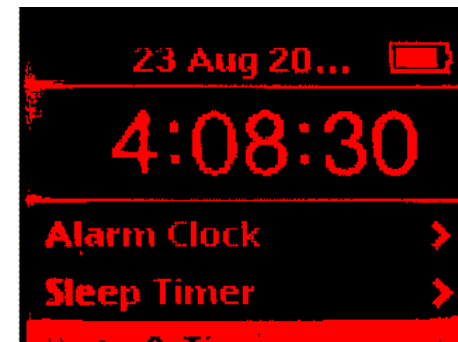
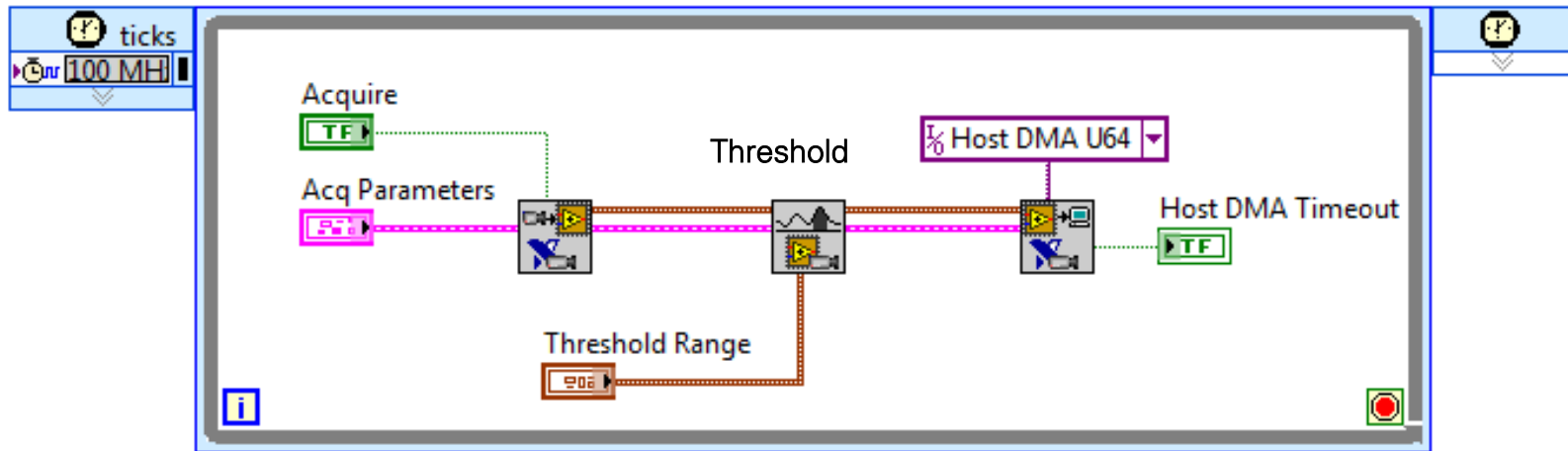
Optical Coherence Tomography



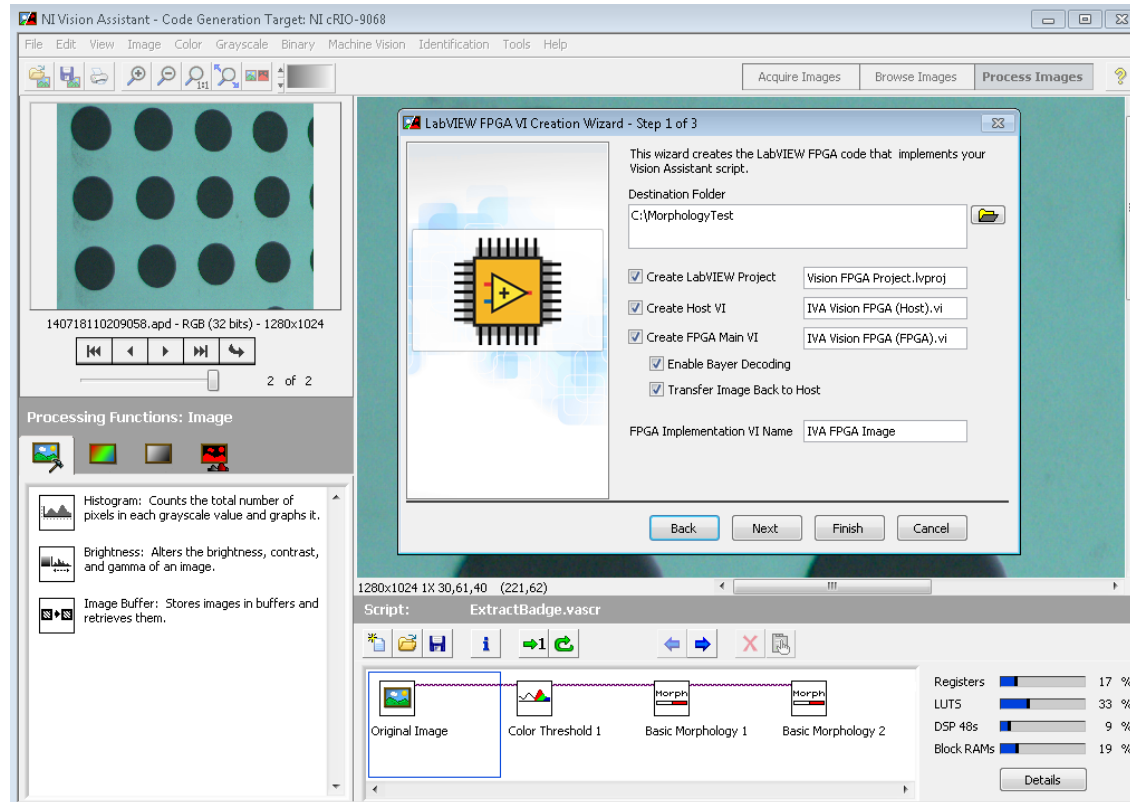
Web & Surface Inspection



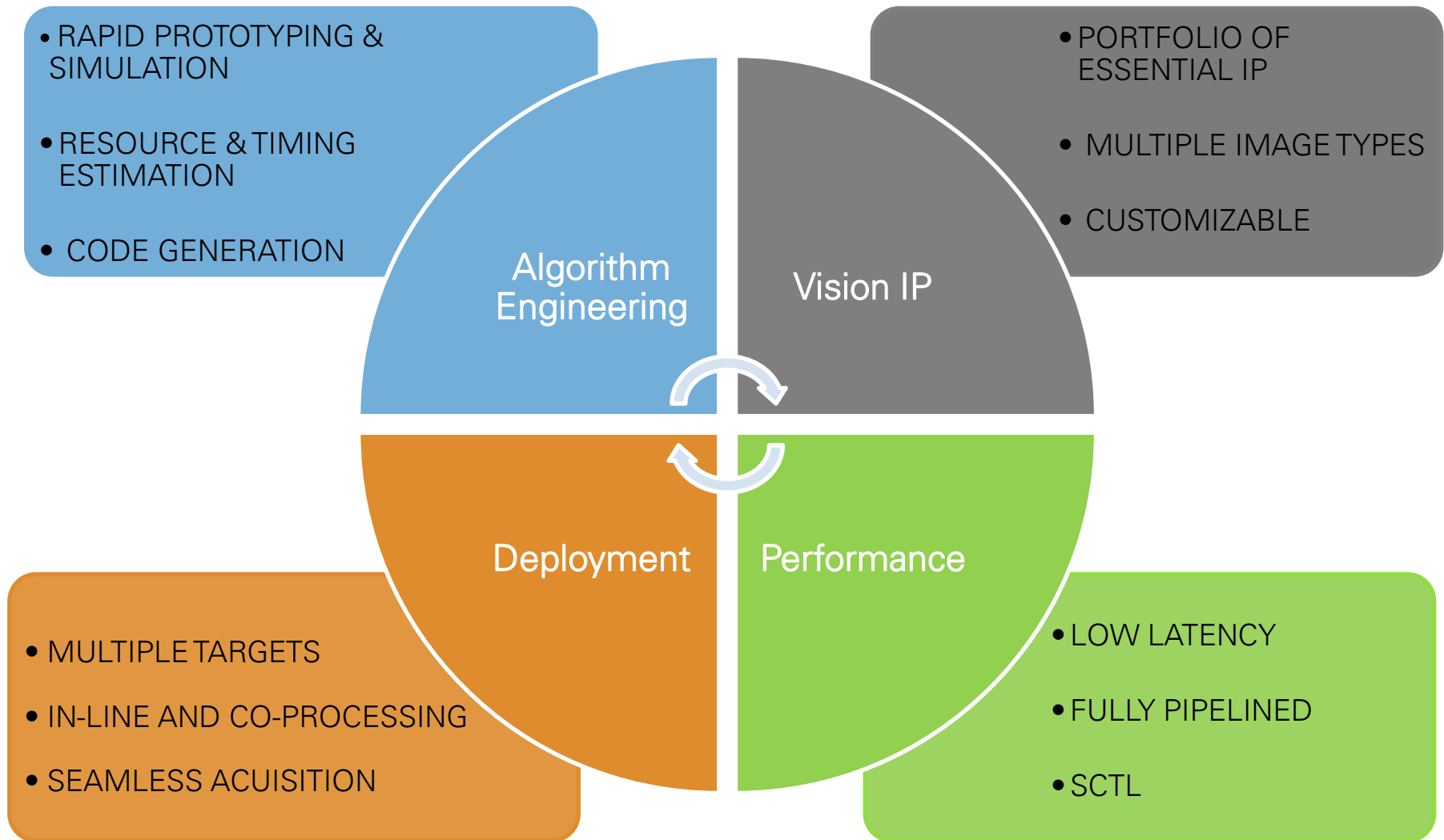
# Pixel Processing Example - Threshold



# From Algorithm Design to Deployment



# NI Vision FPGA Development Platform



# Algorithm Engineering using Vision Assistant

- Rapid prototyping and functional simulation
- Ability to combine IP to design and test a Vision algorithm before compiling the code
- Achieved by:
  - Using Vision Assistant for fast prototyping and code generation
    - FPGA Resources Estimation
    - Automatic parallelization of code
    - Synchronization of parallel streams (latency balancing etc.)
  - Enforcing that all FPGA IP produces the same result as the corresponding VDM function call on the host



NEW IN  
2014

# Vision Assistant FPGA Code Generation

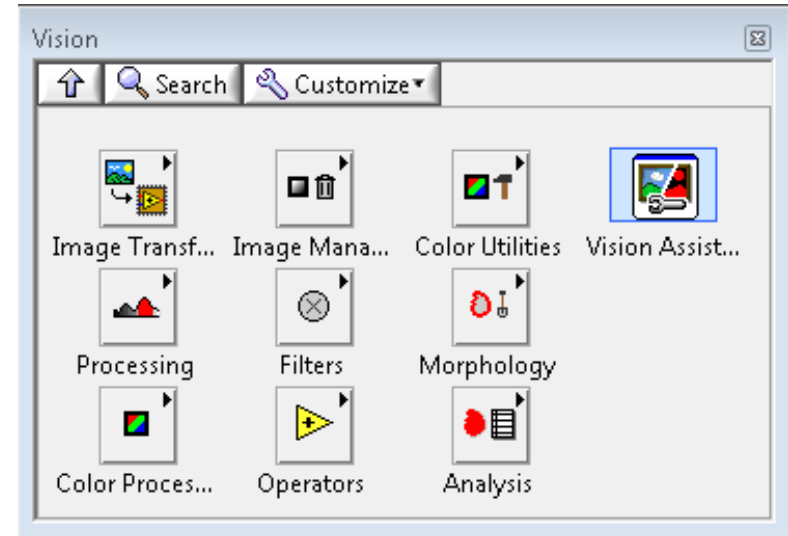
The screenshot displays the NI Vision Assistant interface with the LabVIEW FPGA VI Creation Wizard open. The wizard is in Step 1 of 3 and is configuring the code generation for a script named 'ExtractBadge.vascr'. The destination folder is set to 'C:\MorphologyTest'. The wizard includes options to create a LabVIEW project, host VI, and FPGA main VI, along with checkboxes for enabling Bayer decoding and transferring images back to the host. The FPGA implementation VI name is 'IVA FPGA Image'.

The main interface shows a 1280x1024 image of a grid of black circles on a teal background. Below the image are navigation controls and a 'Processing Functions: Image' panel with options like Histogram, Brightness, and Image Buffer. The script diagram at the bottom shows a sequence of operations: Original Image, Color Threshold 1, Basic Morphology 1, and Basic Morphology 2. Resource usage statistics are shown on the right:

Resource	Usage
Registers	17 %
LUT5	33 %
DSP 48s	9 %
Block RAMs	19 %

# Vision FPGA IP („Intellectual Property“ = functions)

- Efficient Host <-> Target image transfer Vis
- Preprocessing functions
- Support for multiple image types
- Four-wire handshake protocol for streaming
- Synchronization Express VI to support branching and merging
- Partially customizable using IP Builder





# Vision FPGA IP



## Image Management

- Cast
- Vision FPGA Sync



## Color Utilities

- Extract Color Plane
- Bayer to RGB
- RGB to Color
- Color to RGB
- Integer to Color



## Processing

- BCG Lookup
- Inverse
- Threshold



## Filters

- Convolute
- Low pass
- Nth order
- Edge Detection (Sobel, Prewitt, Roberts, Differentiation, Sigma, Gradient)



## Morphology

- Binary (Dilate, Erode, Open, Close)
- Gray (Dilate, Erode, Open, Close)



## Color Processing

- Color Histogram
- Color Threshold

# Vision FPGA IP

## Operators

- Add
- Subtract
- Multiply
- Divide
- Absolute Difference
- MulDiv
- Modulo
- And
- Or
- Xor
- LogDiff
- Mask
- Compare

## Analysis

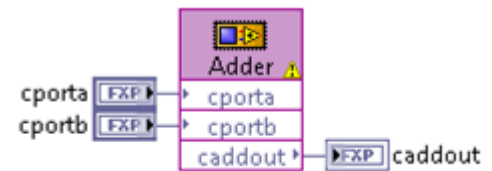
- Histogram
- Quantify
- Centroid
- Linear Averages

## Image transfer

- FIFO to Pixel bus
- Pixel bus to FIFO

# Other Sources for Processing Algorithms

- IPNet ([ni.com/ipnet](http://ni.com/ipnet))
  - Repository for image processing and many other functions
- Xilinx CORE Generator Libraries
  - 15+ blocks for image scaling, color space conversion, noise removal, etc.
  - Integrated within LabVIEW FPGA environment
- IP Integration Node
  - Import custom VHDL to create IP blocks with standard LabVIEW IO interfaces



# Image Processing Functions

## FPGAs not suitable for certain high-level algorithms

- Object-level vision functions
  - Pattern matching
  - OCR/OCV
  - Some geometric measurements
  - Classification



# Vision Assistant FPGA Code Generation

The screenshot displays the NI Vision Assistant interface during the LabVIEW FPGA VI Creation Wizard process. The main window shows a script titled 'ExtractBadge.vascr' with a block diagram containing an 'Original Image' input, a 'Color Threshold 1' block, and two 'Basic Morphology' blocks. A 'Device Utilization Estimate' dialog box is open, providing a detailed breakdown of resource usage for the generated FPGA code.

**LabVIEW FPGA VI Creation Wizard - Step 1 of 3**

This wizard creates the LabVIEW FPGA code that implements your Vision Assistant script.

Destination Folder: C:\MorphologyTest

Create LabVIEW Project: Vision FPGA Project.lvproj  
 Create Host VI: IVA Vision FPGA (Host).vi  
 Create FPGA Main VI: IVA Vision FPGA (FPGA).vi  
 Enable Bayer Decoding  
 Transfer Image Back to Host

FPGA Implementation VI Name: IVA FPGA Image

Buttons: Back, Next, Finish, Cancel

**Device Utilization Estimate**

Steps	Slices	LUTs	DSP 48s	Block RAM
Image Transfer	11519 (32,72%)	10472 (59,5%)	0 (0%)	17 (28,33%)
Histogram 1	122 (0,35%)	234 (1,33%)	0 (0%)	2 (3,33%)
Filters 1	1554 (4,41%)	1357 (7,71%)	1 (1,25%)	3 (5%)
Threshold 1	95 (0,27%)	88 (0,5%)	0 (0%)	0 (0%)
Basic Morphology	773 (2,2%)	704 (4%)	0 (0%)	2 (2,5%)
Basic Morphology	1394 (3,96%)	1301 (7,39%)	0 (0%)	3 (5%)
<b>Total Used</b>	<b>15457 (43,91%)</b>	<b>14157 (80,44%)</b>	<b>1 (1,25%)</b>	<b>26 (44,17%)</b>
<b>Total Available</b>	<b>35200 (100%)</b>	<b>17600 (100%)</b>	<b>80 (100%)</b>	<b>60 (100%)</b>

Buttons: Help, Close

Registers: 17 %  
 LUTs: 33 %  
 DSP 48s: 9 %  
 Block RAMs: 19 %

Button: Details

# FPGA VI

(VI automatically generated by NI Vision Assistant)

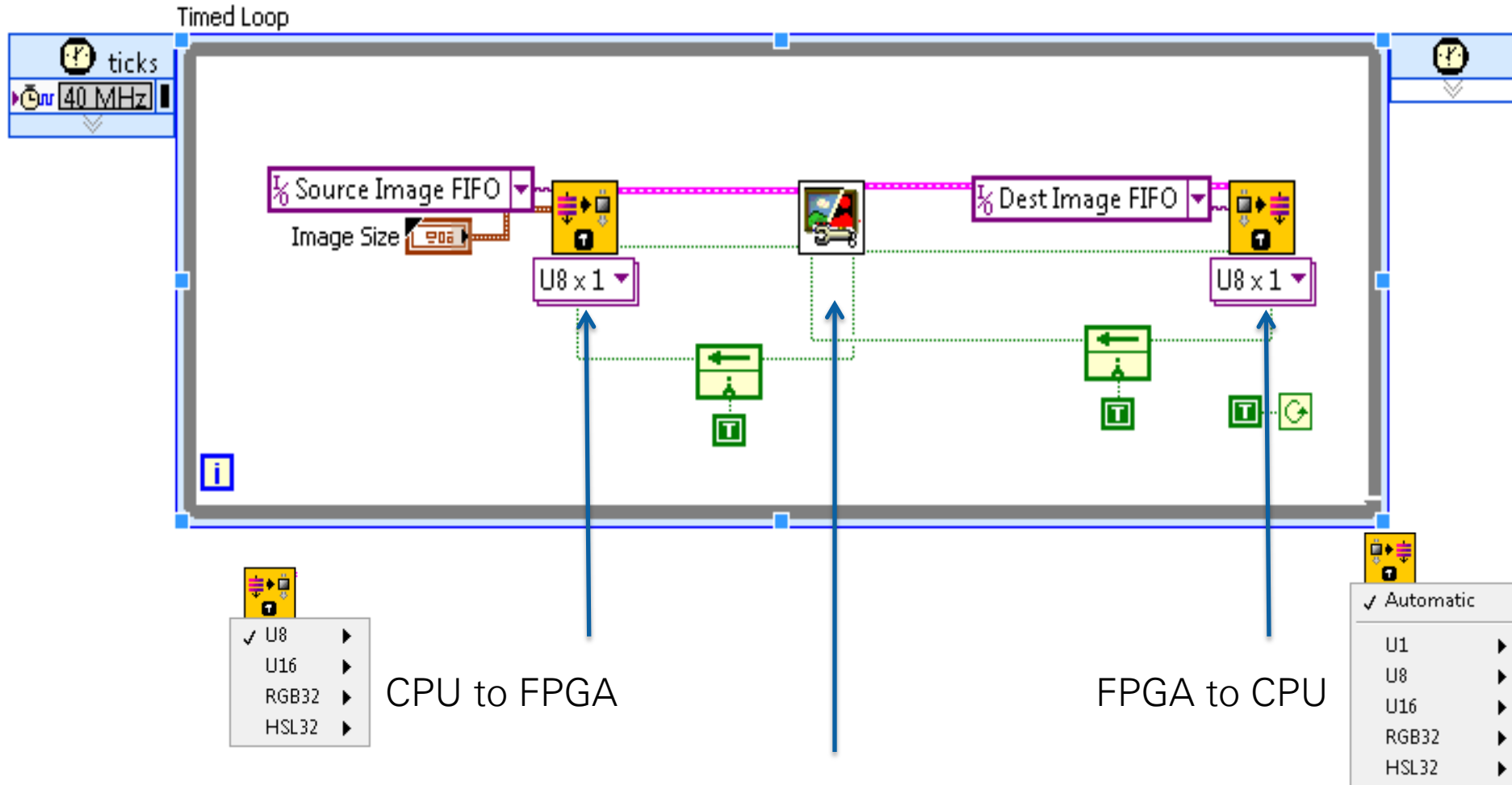


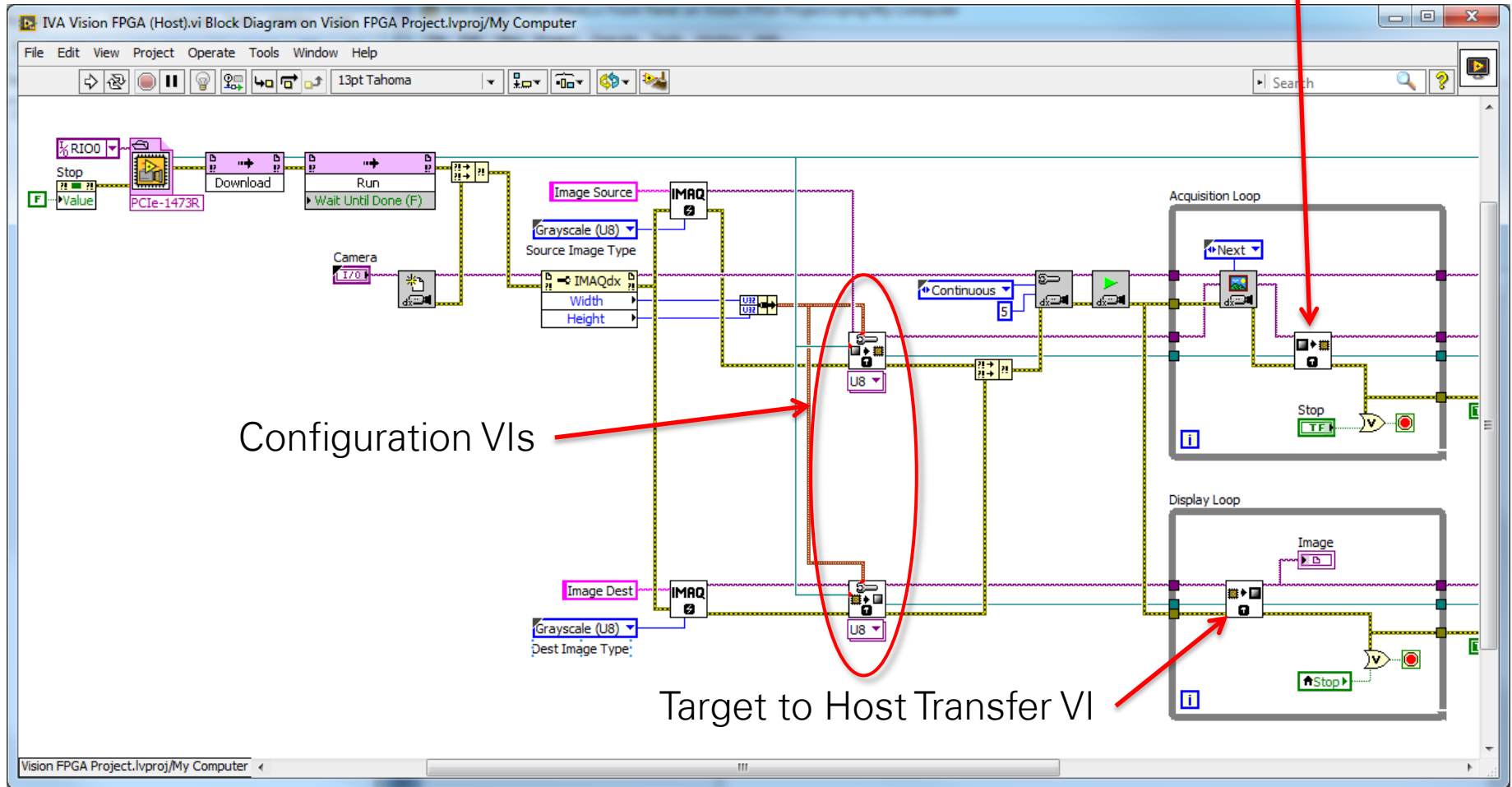
Image Processing



# Host (CPU) VI

(VI automatically generated by NI Vision Assistant)

Host to Target Transfer VI





# Supported Targets

- FPGA Families supported: Zynq™, Kintex, Virtex 5, Spartan 6
- Co-Processing Targets (DMA capabilities, USB/GigE support)
  - NI cRIO (9111, 9112, 9113, 9114, 9116, 9118, 9033, 9034, 9038, 9066, 9067, 9068, 9076, 9081, 9082)
  - NI sbRIO 9606, 9626, 9636, 9651
  - NI myRIO 1900, 1950
  - Compact Vision Systems NI CVS 1457RT, 1458RT and 1459RT
- Inline Processing Targets (Framegrabbers)
  - NI PCIe-1473R-LX50
  - NI PCIe-1473R-LX110



# You Might Want to Use an FPGA for Vision...

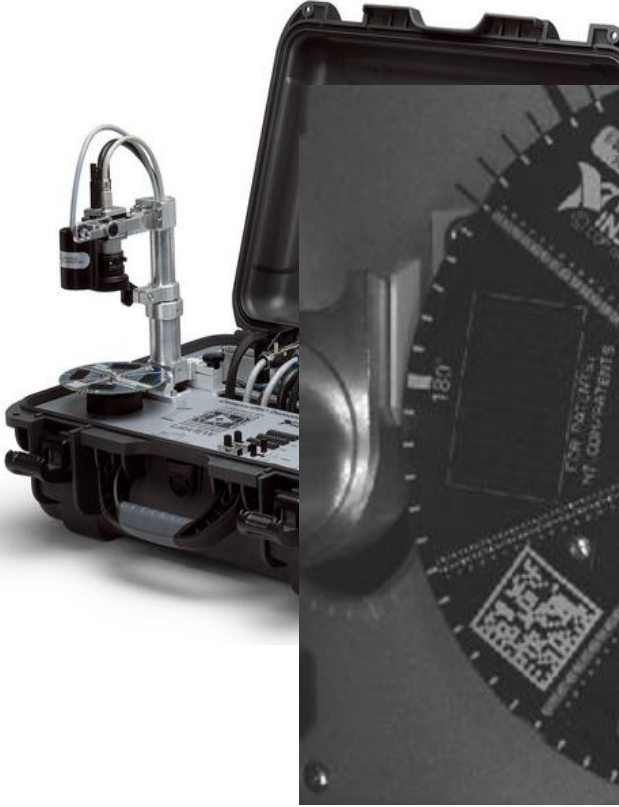
- If latency or jitter is critical
- If power consumption is critical
- If you have to speed up throughput
- If you can pipeline your algorithms
- If you have to reduce the amount of data or aggregate multiple high-speed channels

# Performance Examples

Functions (Number of instances)	CPU (fps)	FPGA (fps)	Speedup	Resources on cRIO – 9068
Convolution Filter (1), Threshold (1), Binary Morphology (1)	23.82	98	4x	LUT – 25% BRAM – 17%
Convolution (10), Operators (4), Morphology (1), Threshold (1)	1.56	98	60x	LUT – 70% DSP – 80% BRAM – 75%

Image Resolution: 640 x 480

# Demo – Rotational Speed control, up to 100fps



VISION MOTION Velocity Control - RT.vi on VisionMotion Velocity Control.lvproj/NI-cRIO-9068-18D9B98...

File Edit View Project Operate Tools Window Help

NATIONAL INSTRUMENTS Vision FPGA Demo POWERED BY NATIONAL INSTRUMENTS LabVIEW™

Enable Motor

Trigger Period (ms)

P

Images per second

Enable Display

Velocity Set Point (rev/sec)

Measured Velocity  rev/s

Processed Image

659x494 16 (5,167)

Measured Velocity

1.05  
1.025  
1  
0.975  
0.95

1234 1334

Time

VisionMotion Velocity Control.lvproj/NI-cRIO-9068-18D9B98 <



Zveme Vás na **NIDays 2014**,  
největší konferenci National Instruments  
v České republice, Praha 22.10. 2014

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Registrace



### NIDays 2014

Nejnovější technologie a trendy v  
navrhování, testování a řízení.



### Datum a čas

22. 10. 2014, 9:00-17:00



### Místo

Hotel Marriott - Praha

Více informací a registrace: [czech.ni.com/nidays](http://czech.ni.com/nidays)

ni.com

