FPGA for image processing

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www.ni.com/vision

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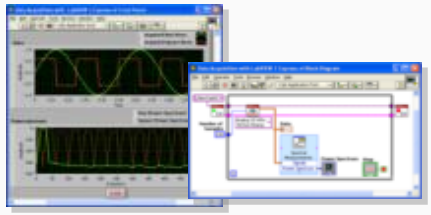
National Instruments - What We Do

NI combines graphical programming software with modular hardware, leveraging the latest technologies.

Low-Cost Modular Measurement and Control Hardware

Productive Software Development Tools



Highly Integrated Systems Platforms

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Graphical System Design

A Platform-Based Approach for Measurement and Control

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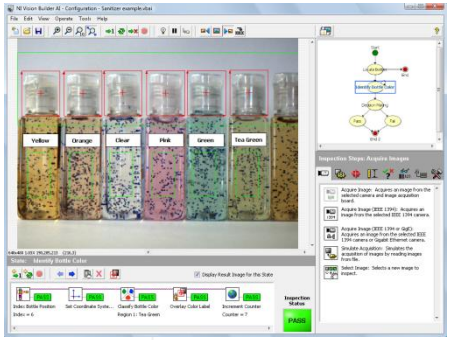
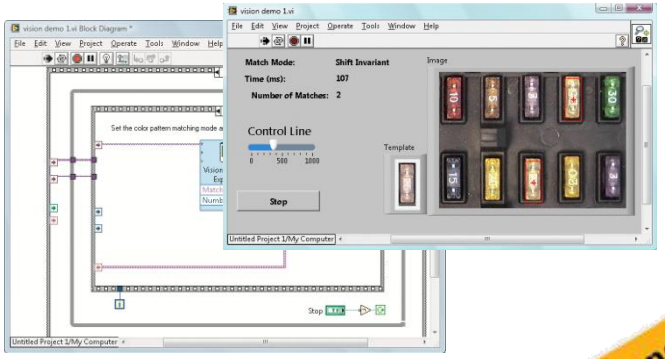
NI Vision Platform





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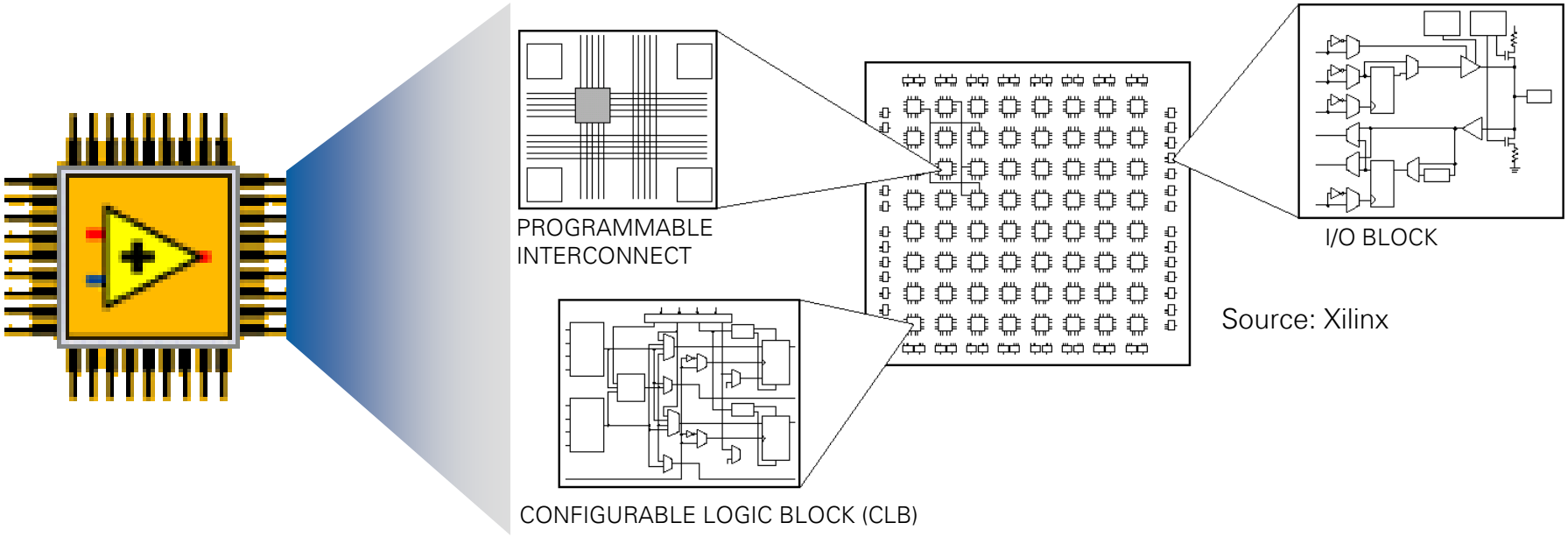
Field Programmable Gate Array (FPGA)

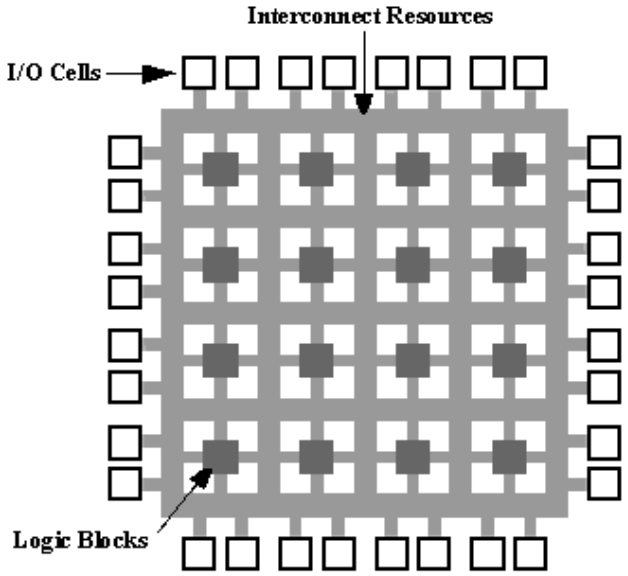


Source: Xilinx

- A semi-conductor device containing many gates (logic devices)
- A wiring list downloaded to the FPGA determines the gate connections and the functionality

FPGAs

- Latency
- Jitter
- Compute power
- Pipelining
- Security
- Weight / Power / Heat
- Complexity
- Raw Clock Rates
- Limited Floating Point support



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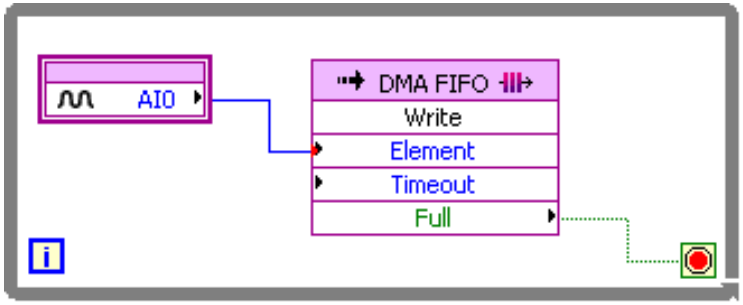
LabVIEW FPGA - Abstraction to the Pin

VHDL



LabVIEW FPGA

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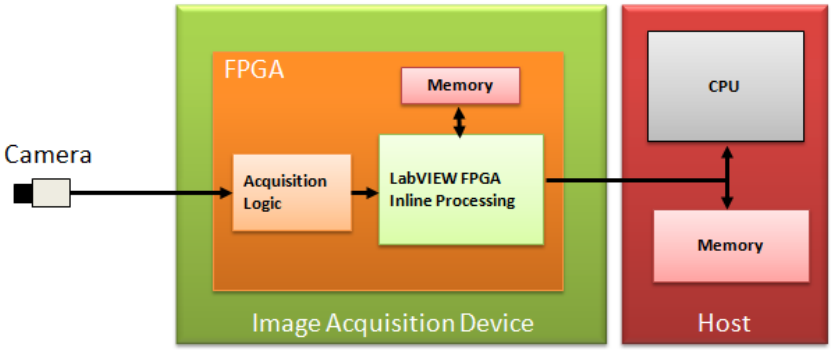
FPGA Image Processing

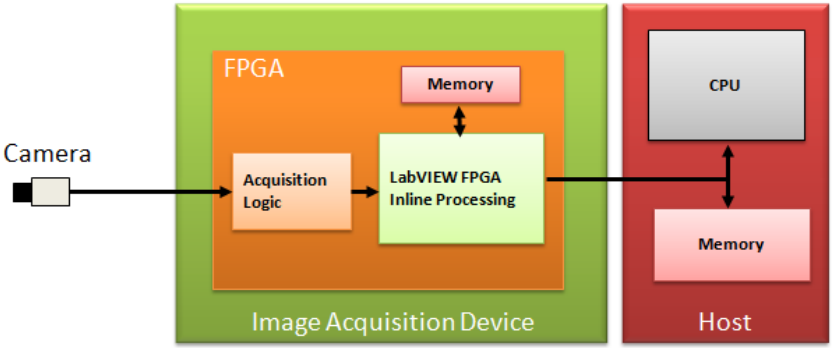
- High-speed control

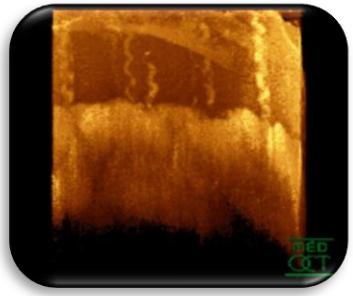


Laser Alignment & Tracking

High-Speed Sorting

- Image pre-processing





Optical Coherence Tomography

Web & Surface Inspection

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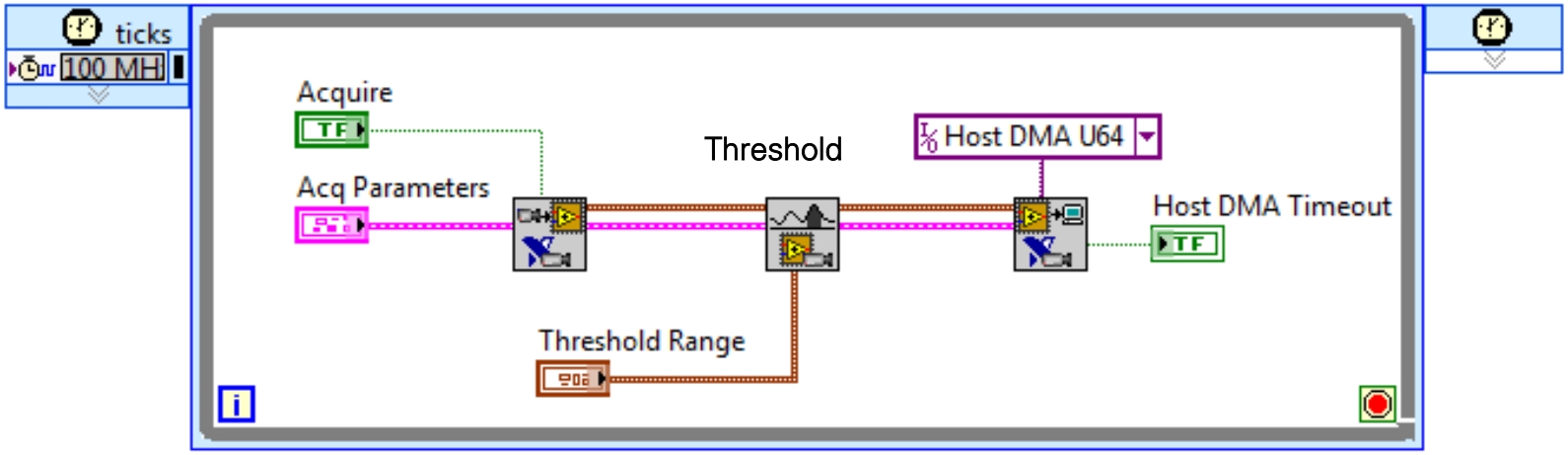
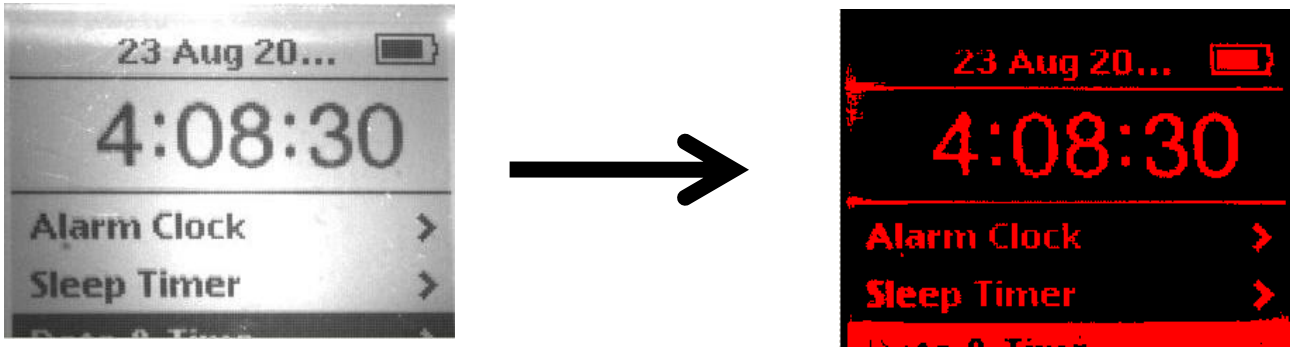
Pixel Processing Example - Threshold





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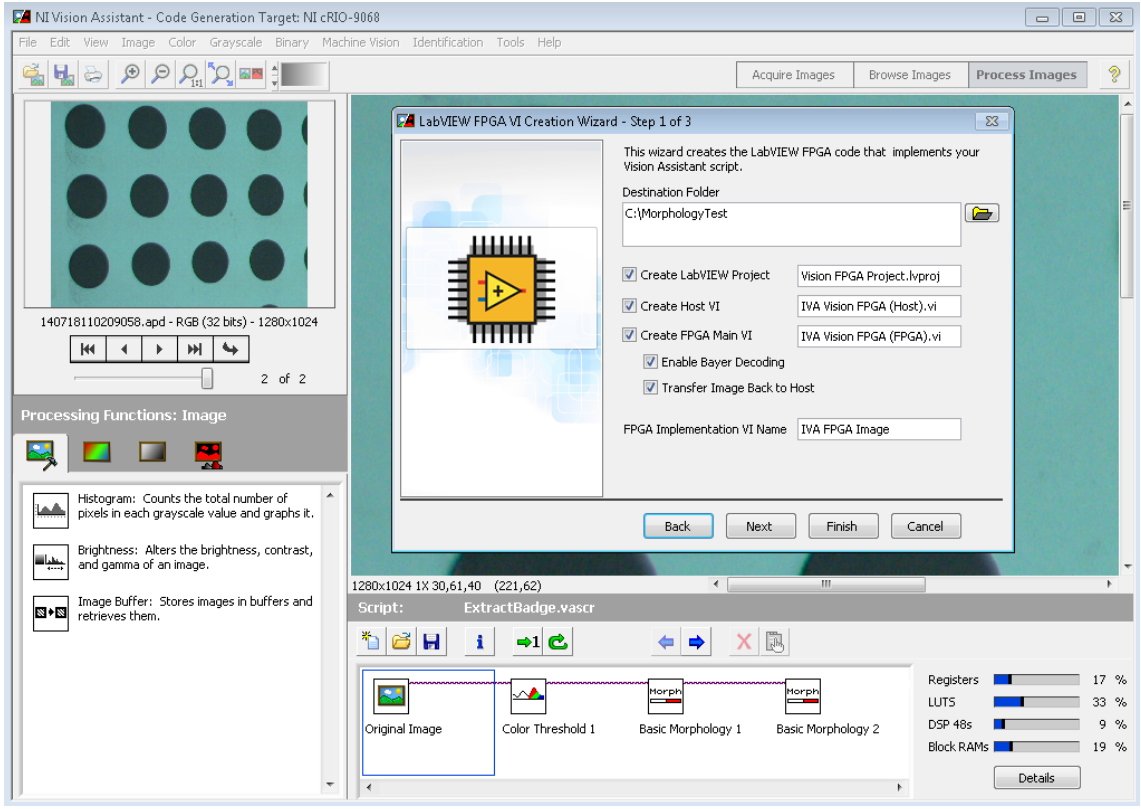
From Algorithm Design to Deployment



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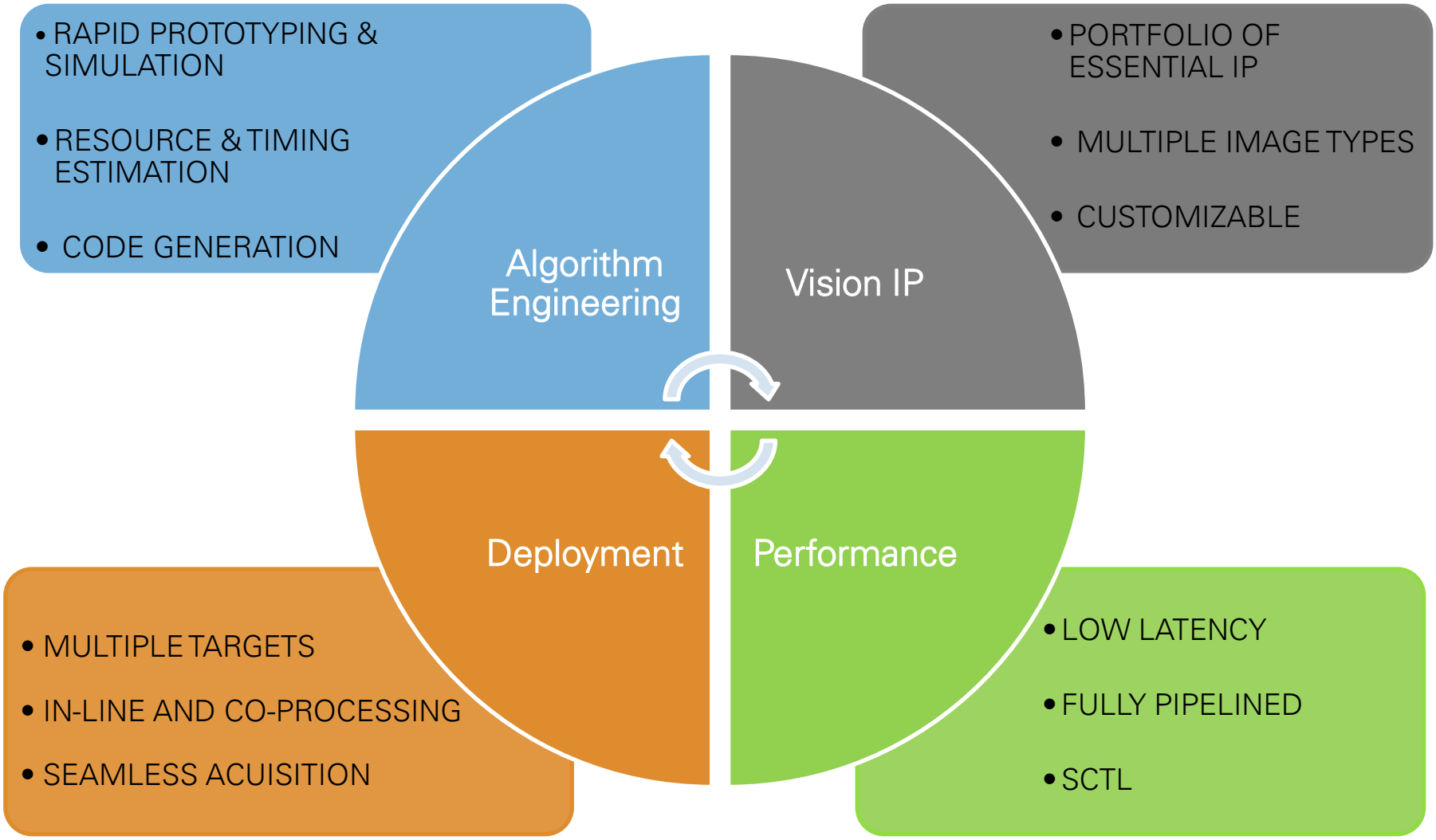
NI Vision FPGA Development Platform



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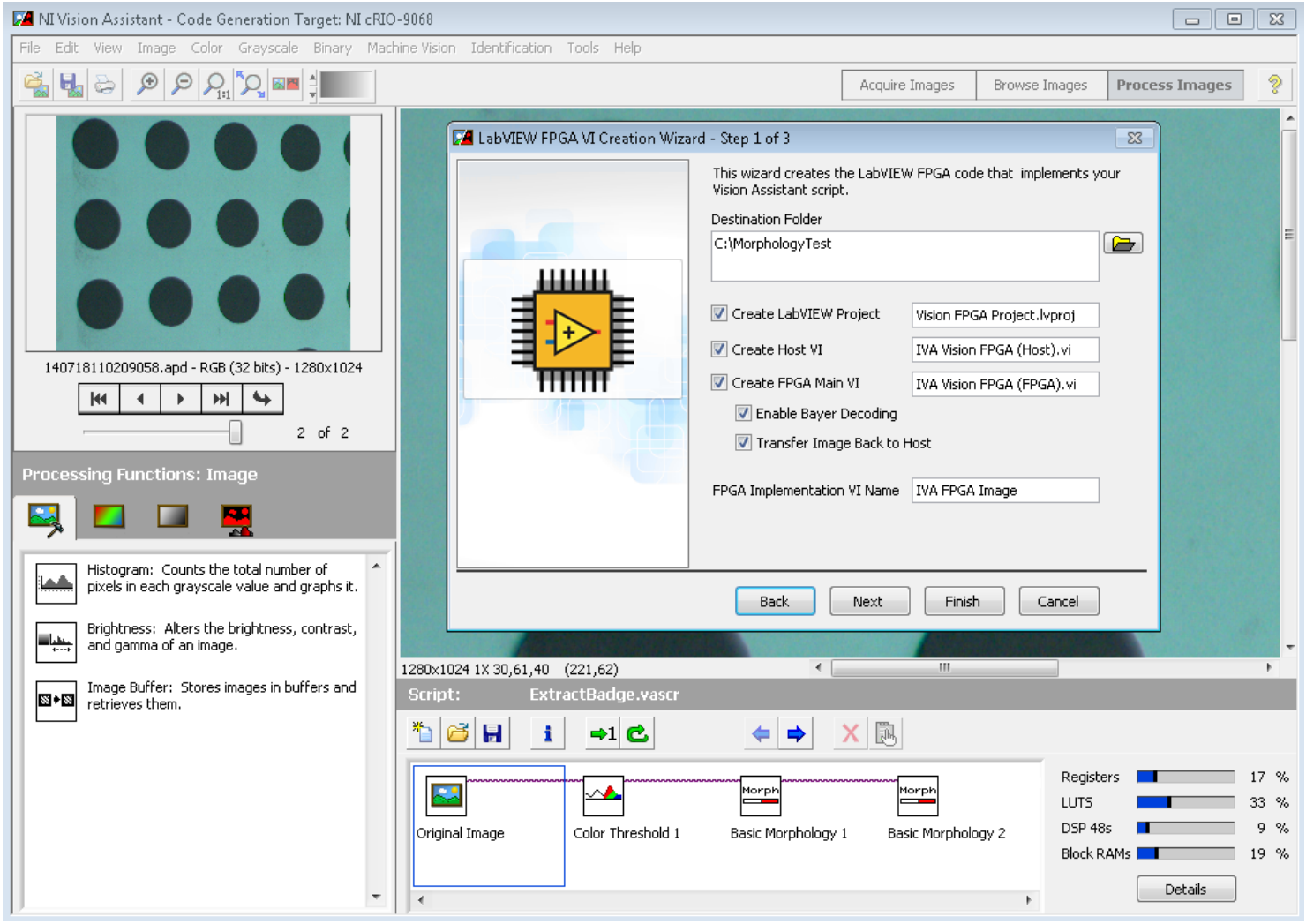
Algorithm Engineering using Vision Assistant

- Rapid prototyping and functional simulation

- Ability to combine IP to design and test a Vision algorithm before compiling the code

- Achieved by:
  - Using Vision Assistant for fast prototyping and code generation
    - FPGA Resources Estimation
    - Automatic parallelization of code
    - Synchronization of parallel streams (latency balancing etc.)
  - Enforcing that all FPGA IP produces the same result as the corresponding VDM function call on the host

Vision Assistant FPGA Code Generation



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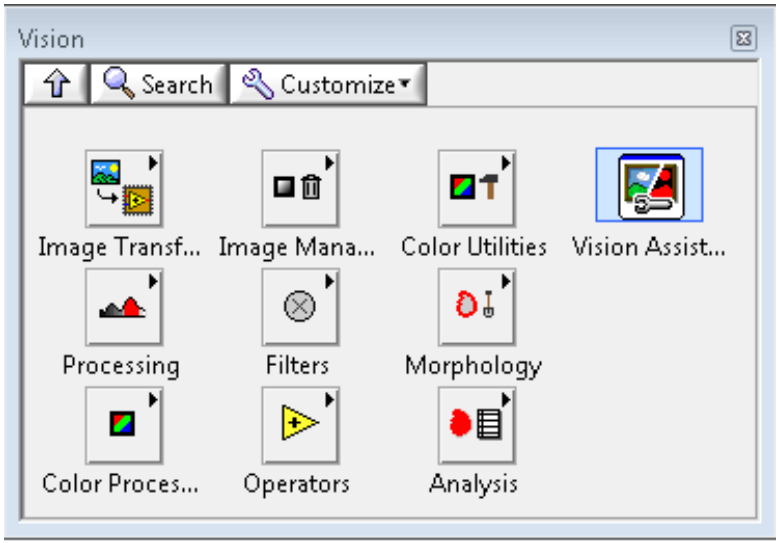
Vision FPGA IP („Intellectual Property“ = functions)

- Efficient Host <-> Target image transfer Vis



- Preprocessing functions
- Support for multiple image types
- Four-wire handshake protocol for streaming
- Synchronization Express VI to support branching and merging
- Partially customizable using IP Builder

Vision FPGA IP

Image Management

- Cast
- Vision FPGA Sync

Color Utilities

- Extract Color Plane
- Bayer to RGB
- RGB to Color
- Color to RGB
- Integer to Color

Processing

- BCG Lookup
- Inverse
- Threshold

Filters

- Convolute
- Low pass
- Nth order
- Edge Detection (Sobel, Prewitt, Roberts, Differentiation, Sigma, Gradient)

Morphology

- Binary (Dilate, Erode, Open, Close)
- Gray (Dilate, Erode, Open, Close)

Color Processing

- Color Histogram
- Color Threshold

Vision FPGA IP

Operators

- Add
- Subtract
- Multiply
- Divide
- Absolute Difference
- MulDiv
- Modulo
- And
- Or
- Xor
- LogDiff
- Mask
- Compare

Analysis

- Histogram
- Quantify
- Centroid
- Linear Averages

Image transfer

- FIFO to Pixel bus
- Pixel bus to FIFO

Other Sources for Processing Algorithms

- IPNet (ni.com/ipnet)
  - Repository for image processing and many other functions
- Xilinx CORE Generator Libraries
  - 15+ blocks for image scaling, color space conversion, noise removal, etc.
  - Integrated within LabVIEW FPGA environment
- IP Integration Node
  - Import custom VHDL to create IP blocks with standard LabVIEW IO interfaces

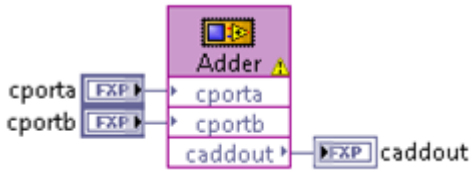


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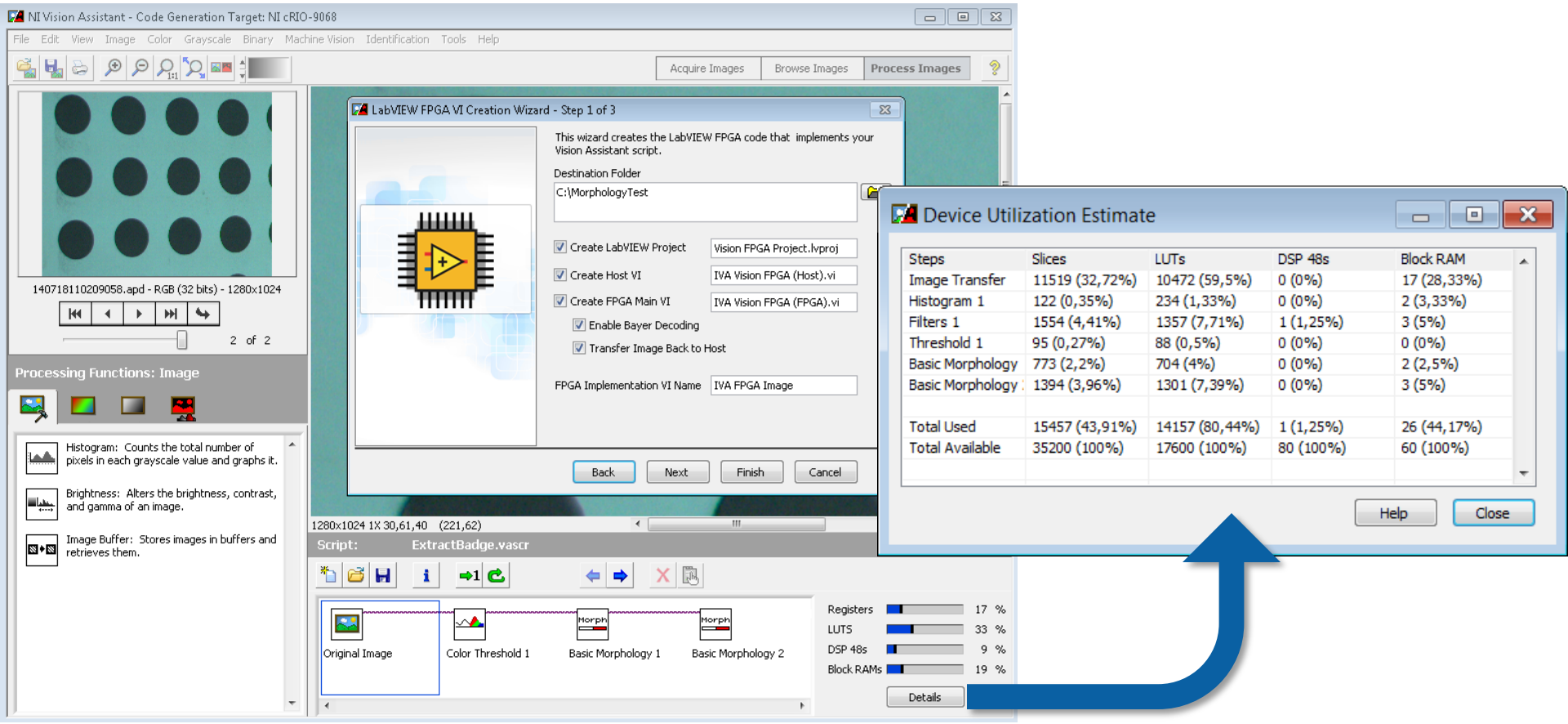
Image Processing Functions

FPGAs not suitable for certain high-level algorithms

- Object-level vision functions
  - Pattern matching
  - OCR/OCV
  - Some geometric measurements
  - Classification

Vision Assistant FPGA Code Generation



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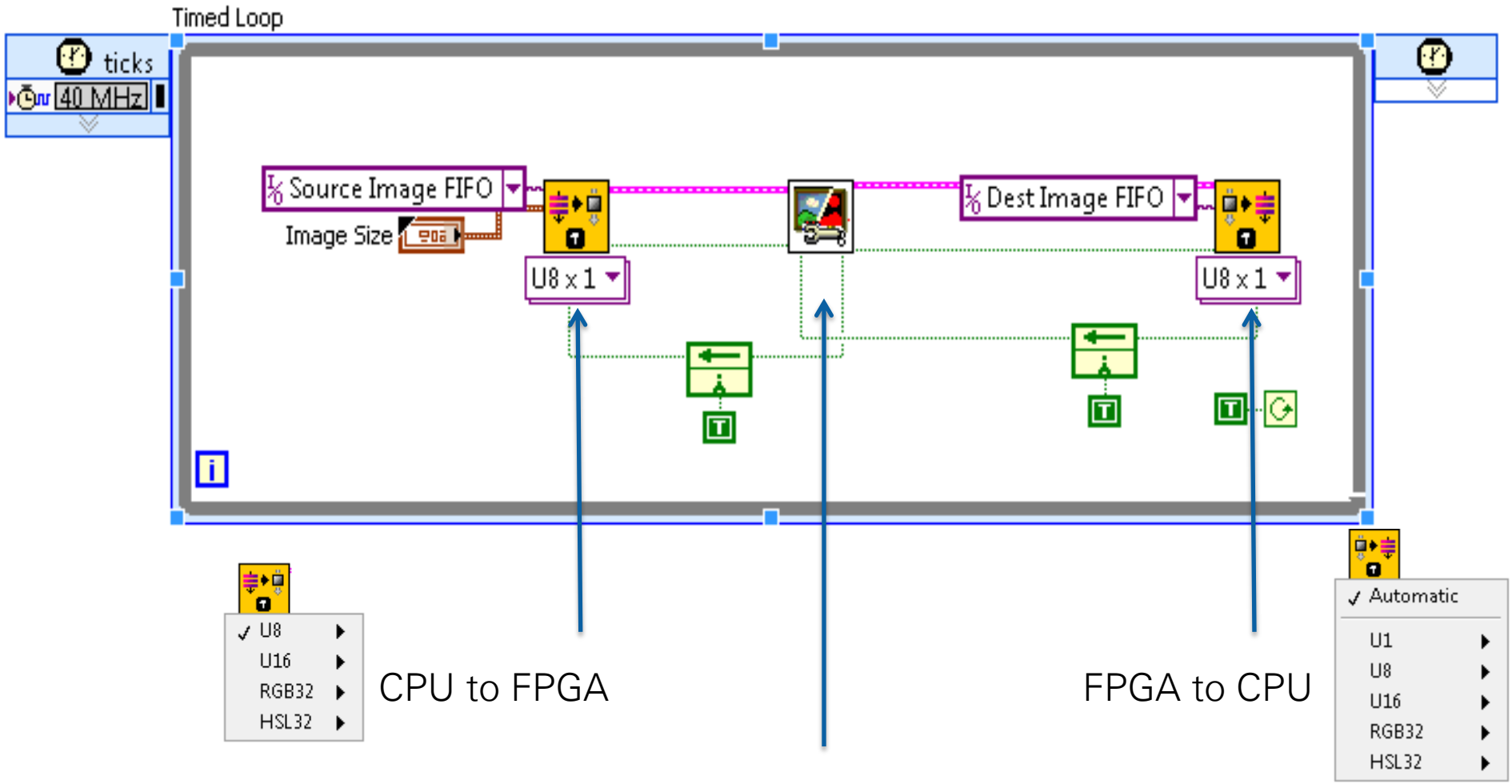
FPGA VI

(VI automatically generated by NI Vision Assistant)



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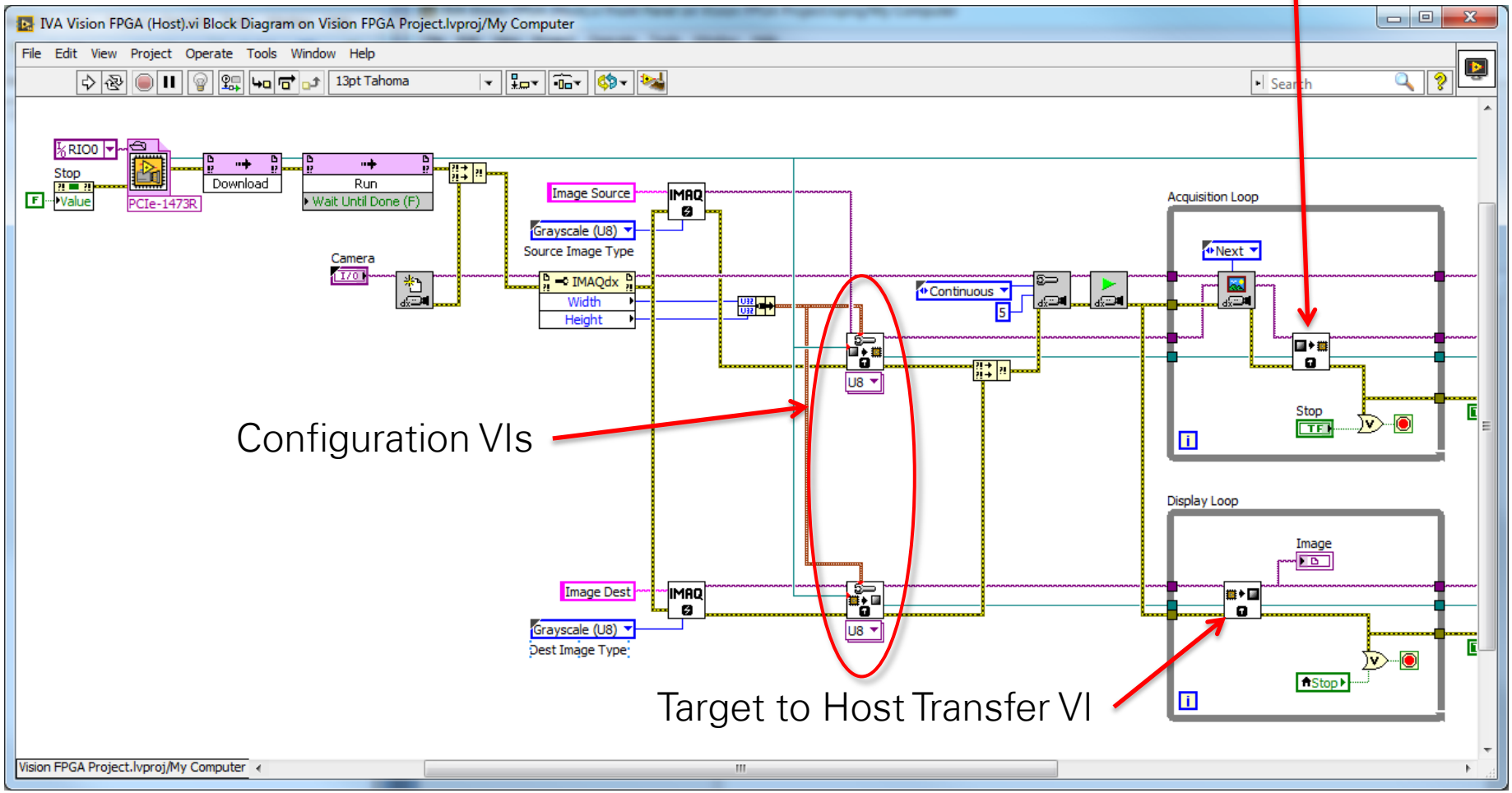
Host (CPU) VI

(VI automatically generated by NI Vision Assistant)

Host to Target Transfer VI



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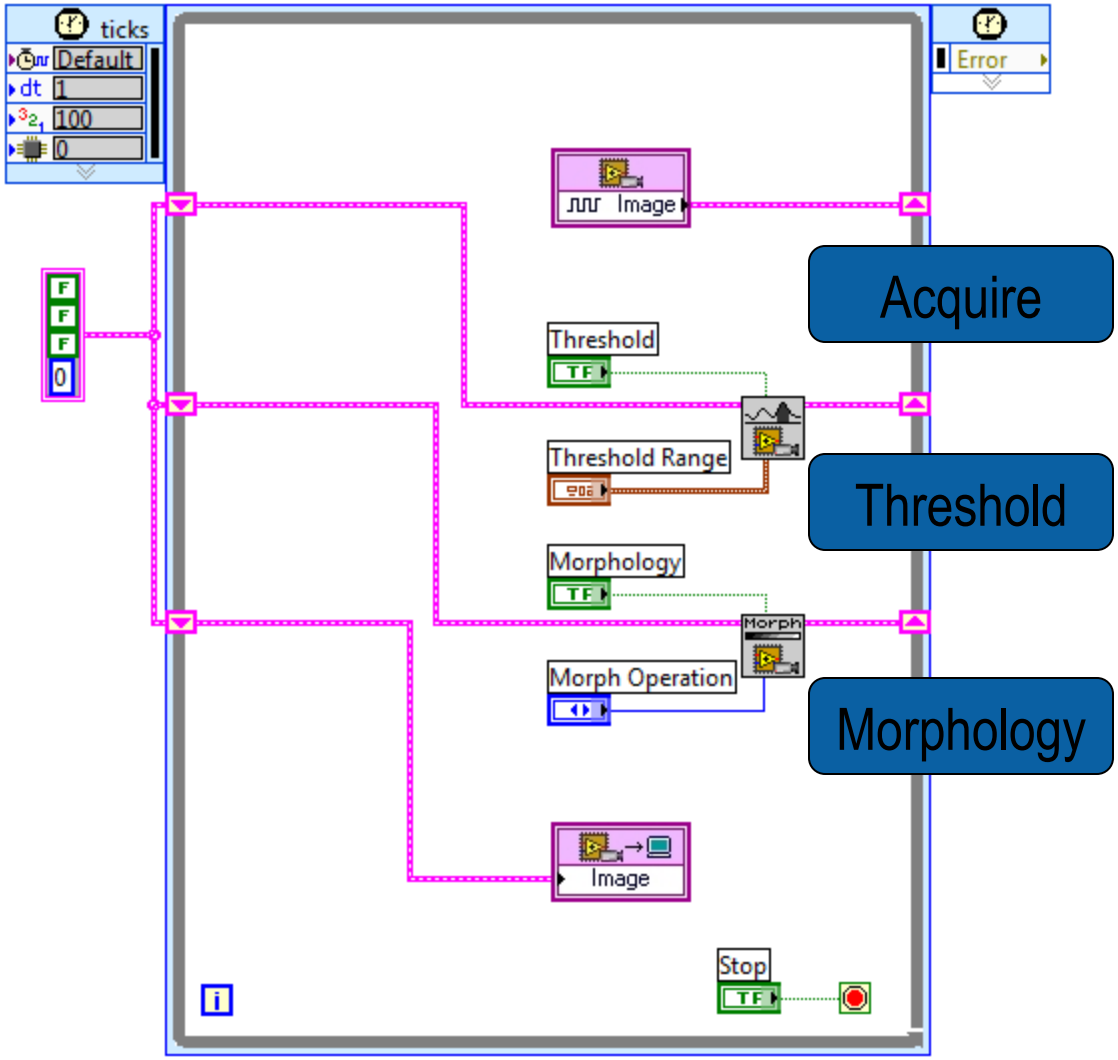
Single Cycle Timed Loop + Pipelining

- Processing loop rate limited by longest delay in loop
- Reduce delays by splitting operations into multiple cycles
- Increases speed, but also latency



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Supported Targets

- FPGA Families supported: Zynq™, Kintex, Virtex 5, Spartan 6
- Co-Processing Targets (DMA capabilities, USB/GigE support)
  - NI cRIO (9111, 9112, 9113, 9114, 9116, 9118, 9033, 9034, 9038, 9066, 9067, 9068, 9076, 9081, 9082)
  - NI sbRIO 9606, 9626, 9636, 9651
  - NI myRIO 1900, 1950
  - Compact Vision Systems NI CVS 1457RT, 1458RT and 1459RT
- Inline Processing Targets (Framegrabbers)
  - NI PCIe-1473R-LX50
  - NI PCIe-1473R-LX110

You Might Want to Use an FPGA for Vision…

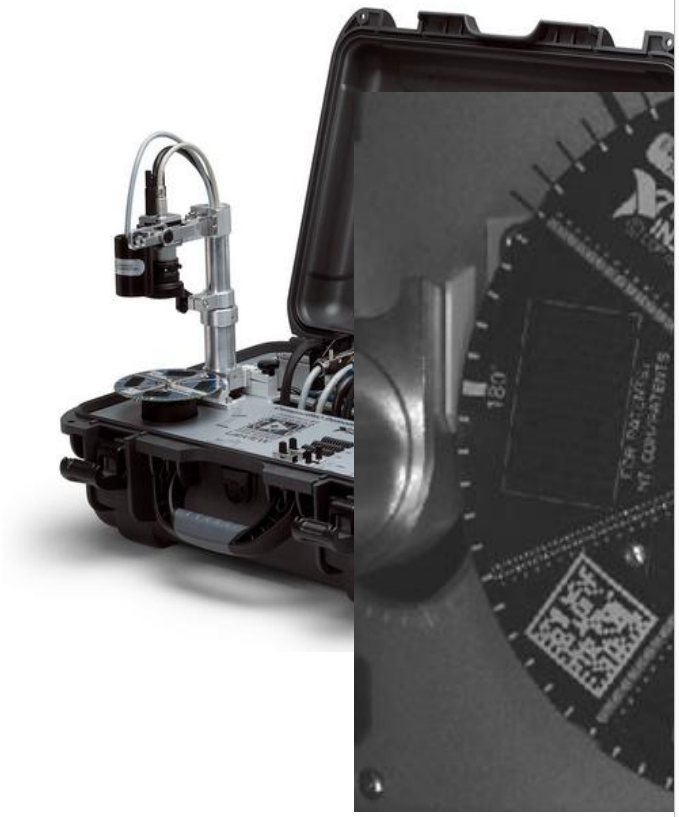
- If latency or jitter is critical
- If power consumption is critical
- If you have to speed up throughput
- If you can pipeline your algorithms
- If you have to reduce the amount of data or aggregate multiple high-speed channels

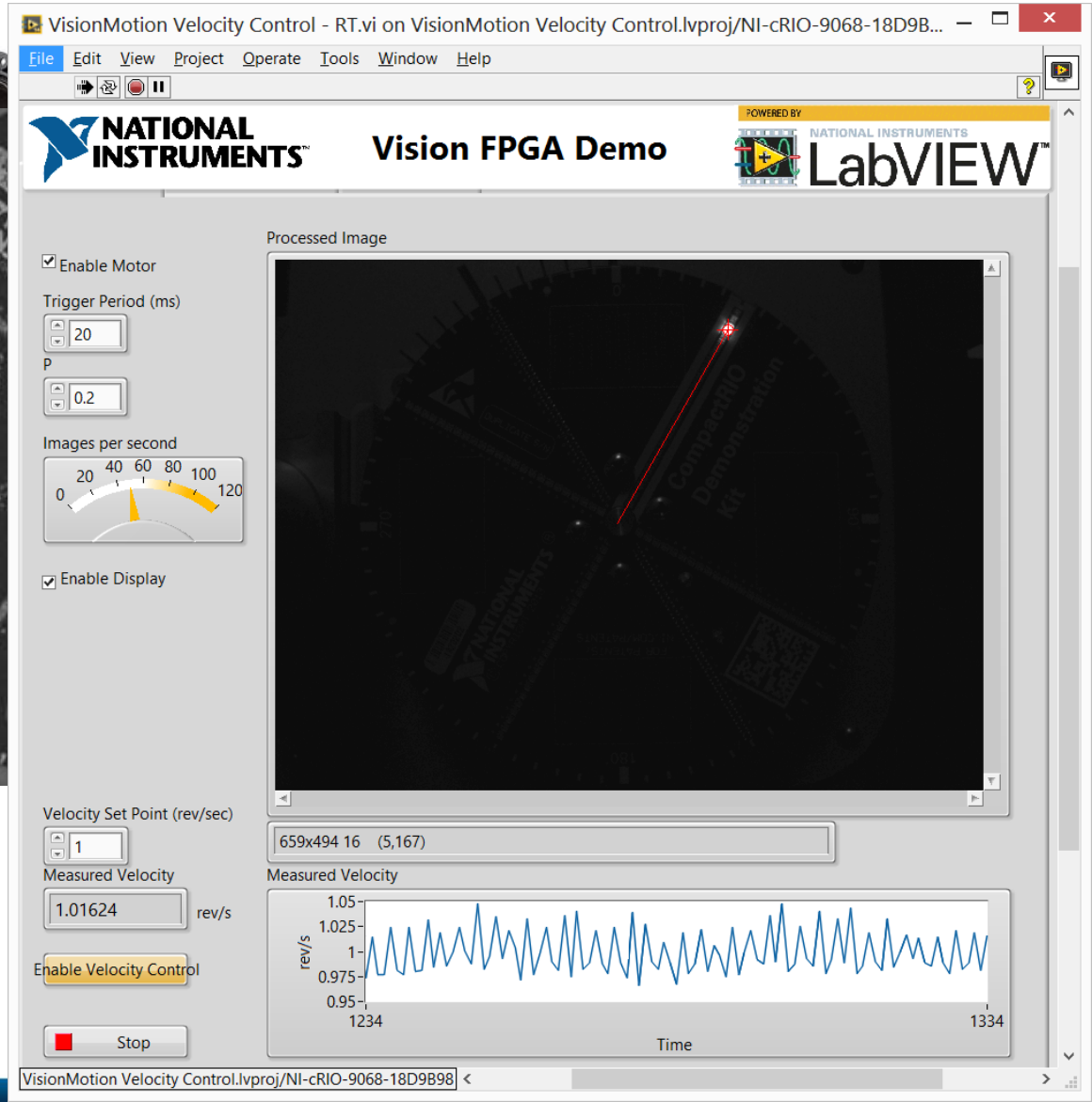
Performance Examples

Functions (Number of instances)	CPU (fps)	FPGA (fps)	Speedup	Resources on cRIO – 9068
Convolution Filter (1), Threshold (1), Binary Morphology (1)	23.82	98	4x	LUT – 25% BRAM -17%
Convolution (10), Operators (4), Morphology (1), Threshold (1)	1.56	98	60x	LUT – 70% DSP – 80% BRAM – 75%

Image Resolution: 640 x 480

Demo – Rotational Speed control, up to 100fps





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Datum a čas

22. 10. 2014, 9:00-17:00

Místo

Hotel Marriott - Praha

Více informací a registrace: czech.ni.com/nidays

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